MODELING, DESIGN, MATERIALS, PROCESSES AND RELIABILITY OF MULTI-LAYER REDISTRIBUTION WIRING LAYERS ON GLASS SUBSTRATES FOR NEXT GENERATION OF HIGH-PERFORMANCE COMPUTING APPLICATIONS

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MODELING, DESIGN, MATERIALS, PROCESSES AND RELIABILITY OF MULTI-LAYER REDISTRIBUTION WIRING LAYERS ON GLASS SUBSTRATES FOR NEXT GENERATION OF HIGH-PERFORMANCE COMPUTING APPLICATIONS

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SUMMARY

There is a growing demand for high performance computing with miniaturization in many electronic systems such as servers for cloud computing, accurate weather prediction, smart mobile and wearable devices and autonomous driving cars. The development of 2.5D silicon interposers in 2010 for heterogeneous integration of graphical processing unit (GPU) to high bandwidth memory (HBM) dies addressed this demand to a certain extent. The back-end-of-line (BEOL) RDL processes in silicon interposers have reached the peak with data rate per signal trace due to the high resistance and capacitance of BEOL RDL, limiting the system bandwidth for 2.5D silicon interposers. The cost of such interposers is also high for large body size substrates (> 1200 sq. mm) due to the fabrication on wafer-based platforms and hence, such interposers have been primarily been used today for cost-insensitive applications like cloud computing. To address these limitations, panel-based organic package substrates with a vast range of body sizes (500-5000 sq.mm) have been under development. These low-cost, high performance panel-based substrates will bring down the cost of high-performance computing systems as well as introduce 2.5D interposers for consumer applications like mobile computing. However, such panel-based substrates have not been able to scale multi-layer polymer RDL below 5 µm RDL which is the primary requirement for 2.5D interposer substrates.

The objectives of this research are to address the scaling limitations of multi-layer polymer RDL down to 2 µm and below. This research is focused on addressing these limitations by: (A) Modeling for layer-to-layer registration to predict the fundamental limit of capture pad required for laminate and glass core substrates (B) Design of multi-layer polymer RDL for 5X bandwidth and 3X lower latency than silicon BEOL RDL (C) Design and demonstration of novel materials

and processes for scaling polymer RDL well below 2 µm using low-cost panel-based tools and processes (D) Reliability analysis of 2 µm multi-layer polymer RDL and identifying future needs for novel polymer dielectrics for scaling polymer RDL to sub 1-micron features.

CHAPTER 1. INTRODUCTION

1.1 Research Background and Motivation

The objective of this research is to model, design, fabricate and characterize for reliability of 2 µm multi-layer redistribution layers (RDL) on glass panel substrates consisting of:

A. Modeling for layer-to-layer registration of multi-layer RDL on glass versus laminate panels

B. Design for 2 µm RDL with superior 5X bandwidth compared to silicon back-end-of-line (BEOL) RDL

C. Materials- Novel ultra-thin polymer dielectrics with the right electrical, mechanical, thermal and chemical properties

D. Processes- Fabrication of high aspect ratio 2 µm copper traces with 2 µm diameter microvias

E. Reliability of 2 µm multi-layer RDL

There has been tremendous amount of research in driving all the technologies for integrated circuit (IC) device scaling since the 1960s. The primary driver for device scaling has been the Moore's Law, which states that the number of transistors in an integrated circuit (IC) doubles every two years [1]. This has resulted in steady increase in transistor density that directly related to increased computing power. Historically, packaging has been defined by Prof Tummala in his 1988 handbook as interconnecting, powering, cooling and protecting the dies [2]. A simple cross-section schematic of a package substrate interconnecting two dies through the printed wiring board (PWB) is shown in Figure 1-1. Thus, the entire system is assembled on to a board which is referred to as System on Board (SoB) in this proposal. As shown in this figure, the redistribution layers

(RDL), consisting of multilayers of conductors and insulators, is the most important aspect of the package substrate that is responsible for interconnecting the dies. As IC device transistor scaling is slowing down in recent times, new solutions are being proposed and investigated to improve performance of the device and the entire system. As per Rock's law, the cost of a semiconductor chip fabrication plant doubles every four years, and this has resulted in slowing down of Moore's law for device scaling along with other physical limitations like scaling to below 3 nm width transistors [3]. With the arrival of smartphones, smartwatches and sophisticated automotive electronics, System on Package (SoP) scaling, pioneered by Georgia Tech, has started gaining global interest in parallel with device scaling. Package substrate has been a huge enabler for system scaling in terms of miniaturization, high bandwidth performance per watt of power consumed and high density of interconnections between heterogeneous dies to enable more operations per second. An example of a SoP system, known as 2.5D substrate, used for high performance computing applications like gaming, deep learning and data centers is shown in Figure 1-2. The term 2.5D refers to interconnecting two or more dies side-by-side on a single package substrate. The short die-to-die interconnect lengths enabled by 2.5D substrates as compared to the traditional 2D substrates shown in Figure 1-1 facilitate superior electrical performance for high performance computing (HPC) systems. A detailed cross-section of the package substrate defining many different aspects of RDL is shown in Figure 1-3. The focus of this research includes build-up RDL which include dielectrics and conductor structures like lines, microvias and capture pads.

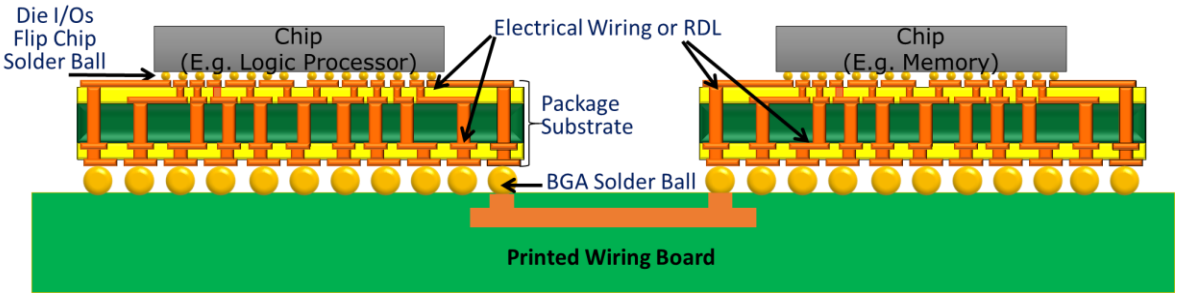


Figure 1-1: Concept of SoB: Schematic of a 2-D package substrate interconnecting two dies through the printed wiring board.

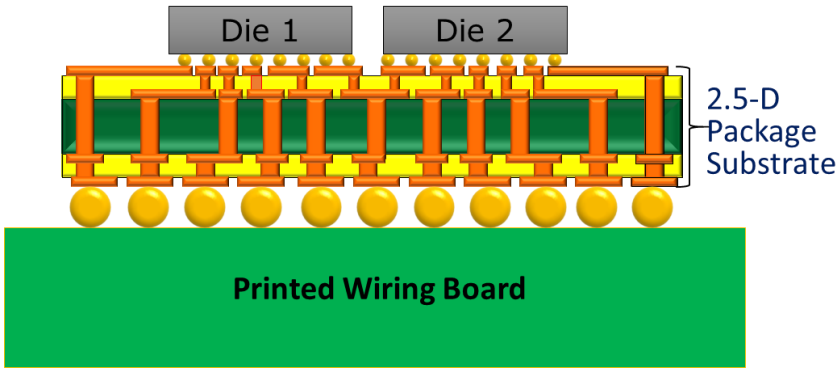


Figure 1-2: Concept of SoP: Schematic of a 2.5D package substrate interconnecting two dies on the package substrate.

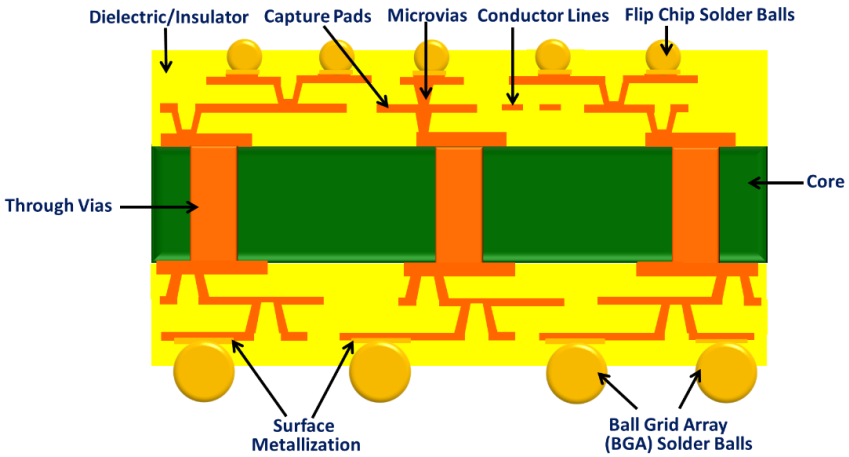


Figure 1-3: RDL technologies: Conductors- Lines, Microvias, Capture Pads and Dielectrics

There are two technologies being pursued to fabricate high-density RDL layers: (A) Back End of Line (BEOL) processes for 300 mm wafer-based platforms with inorganic dielectrics like SiO_2, and (B) Semi-Additive Processes (SAP) that include 500 mm panel-based organic laminate package substrates and 300 mm wafer-based embedded fan-out package substrates with polymer dielectrics. BEOL processes with 1-2 µm RDL wiring at aspect ratios of 0.5-1 suffer from high resistance of copper lines and high capacitance from high D_k (~3.9) of SiO_2 dielectrics. This leads to a high RC delay and limits the system bandwidth of silicon substrates. Panel-based RDL has lower capacitance due to low D_k polymer dielectrics and lower resistance with thick copper line RDL. Thus, polymer RDL has the potential for higher bandwidth, lower RC delay than silicon BEOL RDL. However, semi-additive processes with 500 mm panel-based organic laminate panels have been limited to 6 µm RDL wiring with 20 µm diameter microvias and 32 µm diameter capture pads, far below the wiring densities required to interconnect multiple dies for 2.5D substrates [4]. The dimensional instability of laminate panels leads to large capture pads, limiting the wiring density. Embedded wafer-level fan-out package substrates have been prototyped to scale to 2 µm RDL with spin-on polymer dielectrics [5]. The aspect ratios of fine pitch copper wiring with polymer RDL have been limited to 1 due to challenges in the isotropic seed layer etch process. This limits the flexibility to design an electrical system with polymer RDL having superior bandwidth than silicon BEOL RDL. Also, interfacial delamination of high aspect ratio, narrow width (< 4 µm) copper wiring from polymer dielectrics is a concern. In terms of reliability of multi-layer RDL with polymer dielectrics, there have been limited materials and processes to scale microvia diameters below 10 µm [[6],[7]]. This limits the scaling of I/O density with polymer RDL. The electrical leakage reliability failures between fine pitch RDL wiring due to moisture absorption of polymer dielectrics have also limited the scaling down of polymer dielectric RDL

below 5 µm [8]. Thus, there is a critical need to scale polymer-based panel RDL to 2 µm with improved materials and processes and with superior reliability, enabling improved electrical performance than silicon BEOL at similar I/O wiring densities. This research will enable high density 2 µm multi-polymer RDL with 5X higher bandwidth and 3X lower latency with lower energy per bit than silicon RDL for high performance computing applications.

This research addresses the challenges to achieve this goal with five major objectives:

(A) Study the fundamental limit of laminate versus glass panels to predict the minimum capture pad required for landing a 2 µm microvia

(B) Optimize the design for 2 µm half-line pitch RDL to achieve superior bandwidth for panel RDL with polymer dielectrics compared to silicon BEOL RDL

(C) Design and develop advanced materials to fabricate 2 µm multi-layer polymer RDL

(D) Develop novel advanced processes to fabricate 2 µm multi-layer polymer RDL

(E) Study reliability of fabricated 2 µm multi-layer polymer RDL.

The I/O bump pitch of high-performance computing dies are expected to shrink to 10 µm in the next five to ten years. The cross-section of 2 µm polymer RDL technology with summarized research challenges is shown in Figure 1-4. This polymer RDL technology can be scaled to I/O bump pitch as small as 10 µm.

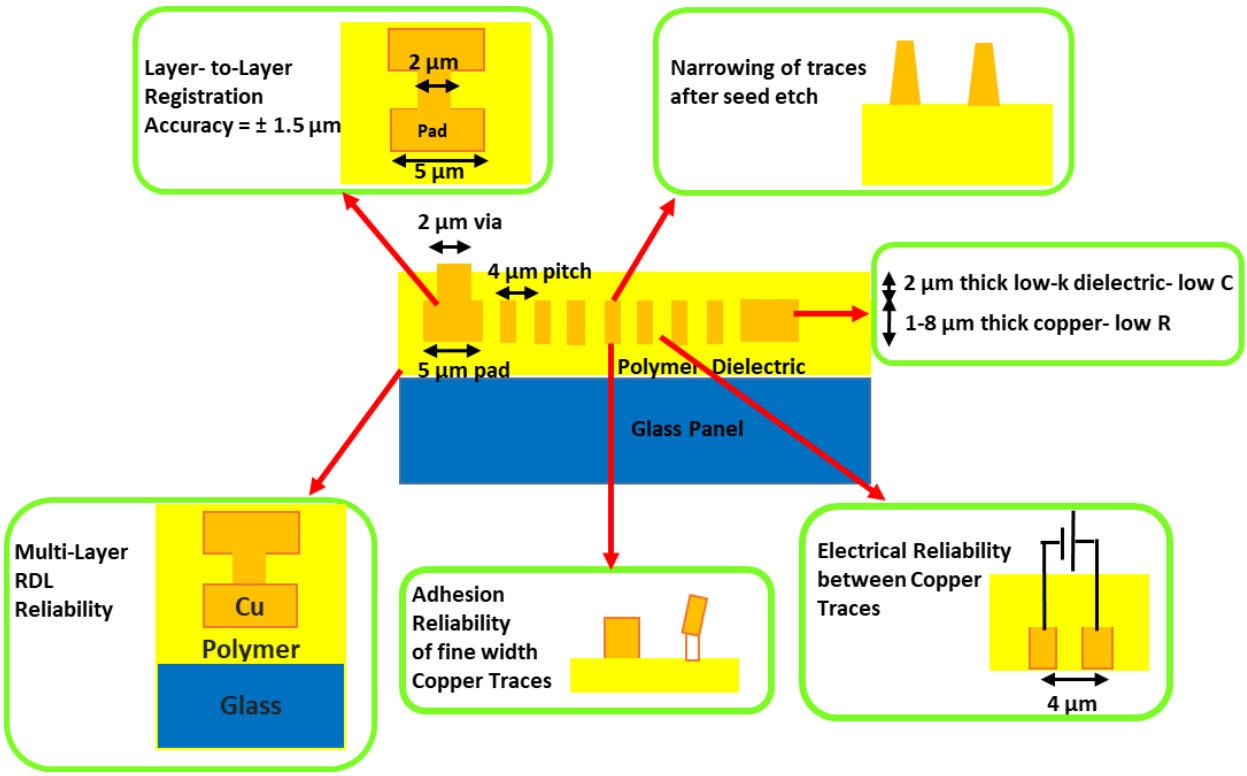


Figure 1-4: Future 2 µm multi-layer polymer RDL stack-up for 2.5D glass panel with research challenges

1.2 Current State-of-the-Art RDL Technologies and their Limitations

The proposed research addresses the challenges in modeling, design, materials, processes and reliability of multi-layer RDL for panel substrates:

1.2.1 Modeling for layer-to-layer registration

The critical aspect of designing 2 µm multi-layer RDL is the diameter of the capture pad required to land a microvia. I/O wiring density for any specific RDL technology is defined by the line width (L) and space (S), the capture pad diameter (D) required to land a microvia and is normalized for a certain bump pitch (P) of the die as given in equation 1-2 below. In equation 1-1

below, ‘n' refers to the number of rows of bumps that can be routed in one metal layer of the RDL assuming L and S to be equal [9].

$$n = \{[(P-D)/W] - 1\}/2 \quad \textbf{Eq. (1-1)}$$

$$\textbf{I/O density in terms of IOs/mm/layer} = (n+1)/P \quad \textbf{Eq. (1-2)}$$

The calculations are as shown below in Table 1-1 which clearly highlight the significance of capture pad diameter. As capture pad diameter increases from 5 µm for BEOL RDL with 2 µm L/S to 25 µm for hybrid RDL with similar 2 µm L/S, the I/O density decreases from ~235 to ~135 IOs/mm/layer. Figure 1-5 shows the simplified view of current panel SAP RDL with one copper line (n=1) routed between two capture pads.

The current organic laminate panels require 25 µm diameter capture pads to land 10 µm microvia diameters [6]. Laminate panels have lower elastic modulus and poor dimensional stability during thermal processing. This results in a need to have large capture pads, limiting the wiring density. Package substrate RDL is fabricated using a sequential approach which requires curing of polymer dielectric [typically around 200 ^{0}C] for every layer and the dimensional instability of laminate core panel causes the capture pads to shift from their original location in the RDL. Thus, capture pads larger than the diameter of microvias are required to land the microvia, severely restricting the space available for routing copper lines to connect the die bumps. The research proposed here uses a glass panel core for smaller capture pads due to its excellent dimensional stability similar to that of silicon. This research will demonstrate modeling and characterization of layer-to-layer registration shifts for organic laminate and glass core panels.

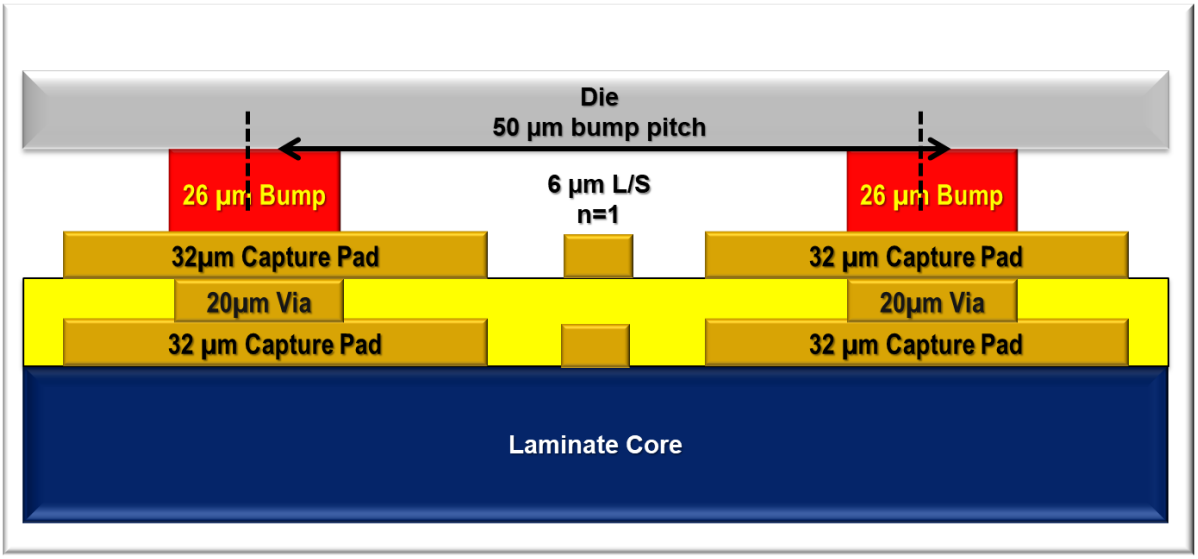


Figure 1-5: Current SAP RDL with one copper line (n=1) routed bwtween two capture pads using panel laminate core

Table 1-1: Comparison of I/O densities for different RDL technologies and significance of capture pad diameter in scaling I/O wiring densities

No.	Parameters	BEOL RDL (300 mm wafer)	SAP RDL (500 mm large panels)	Hybrid RDL SAP + BEOL
1	Line Width (L) /Spacing (S)	2/2 µm [10]	6/6 µm [4]	2/2 µm [6]
2	Microvia Diameter/ Capture Pad (D)	2/5 µm	20/32 µm [4]	10/25 µm [6]
3	Bump Pitch (P)	50 µm	50 µm	50 µm
4	No. of routed rows (n)	~ 11	~ 1	~ 6
5	I/O wiring density in terms of IOs/mm/layer	~ 235	~ 40	~ 135

1.2.2 Design for 2 µm high bandwidth, low RC delay (where R- resistance and C-capacitance) RDL

BEOL RDL is the only RDL technology today that can meet the required I/O densities. However, the low aspect ratio copper lines of silicon BEOL RDL combined with high dielectric constant of SiO_2 limit the signal data rate and system bandwidth of 2.5D silicon package substrates. Therefore, most of the electrical design models have focused on signal data rates (2-4 Gbps per copper line) at lower frequencies [below 2 GHz] for high performance computing systems. A summary of this model showing the significance of polymer RDL in terms of RC delay is shown in Figure 1-6 [11]. However, the goal of polymer RDL is to scale signal data rates greater than 10 Gbps per copper line and improve system bandwidth. At higher frequencies (> 5 GHz) with the typical line lengths of 1-6 mm for copper lines, these lines should be modeled as transmission lines [12]. This research will model commonly used stripline and embedded microstrip transmission lines at higher frequencies to predict the optimum aspect ratios of copper lines at 4 µm pitch and optimum thicknesses of polymer dielectrics to enable higher bandwidth 2.5D glass package substrates.

	Polymer 1	Polymer 2	SiO2
Width (µm)	10	10	1.2
Spacing (µm)	10	10	0.8
Length (cm)	1	1	1
Thickness (µm)	3	3	1
Height (µm)	3	10	1
Relative permittivity	3	3	3,9
R (Ohm/mm)	0.733	0.733	18
C (fF/mm)	187	113	246
RC-delay (ps/cm)	1.37	0.83	44.28

Figure 1-6: RC delay for polymer RDL versus inorganic SiO_2 BEOL RDL [11]

1.2.3 Materials

An ideal polymer dielectric material has to have the right electrical, mechanical, thermal and chemical properties for the given application. Traditional packaging polymer dielectrics like epoxies have been suited for > 10 µm RDL with aspect ratios of 1. With the advent of embedded fan-out package architectures, novel polymer dielectrics with improved properties were developed to scale to < 10 µm RDL. The current status of the properties of different types of polymer dielectrics is summarized in Figure 1-7 [13]. These properties will be used as benchmark to design polymer dielectric materials with the right set of properties for reliability of RDL with 2 µm L/S and below 5 µm microvia diameters. The proposed research also addresses metal-polymer interfacial adhesion in scaling to high aspect ratio RDL. Interfacial adhesion of metal seed to polymer dielectrics is a critical challenge as aspect ratios of copper lines become higher and novel low-k, non-polar, smooth polymer dielectrics are being developed. The proposed research addresses metal-polymer interfacial adhesion by characterizing different polymer dielectric chemistries and predicting ideal functional groups to enhance metal-polymer bond strengths.

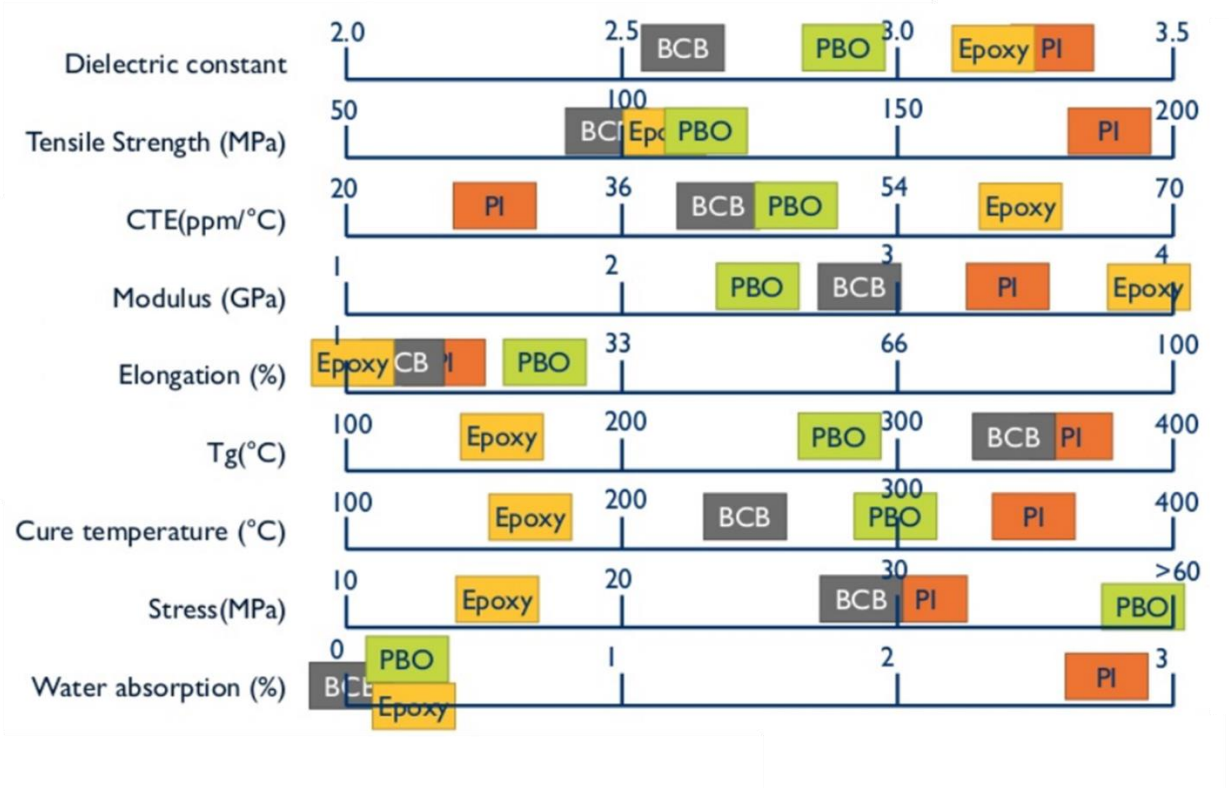
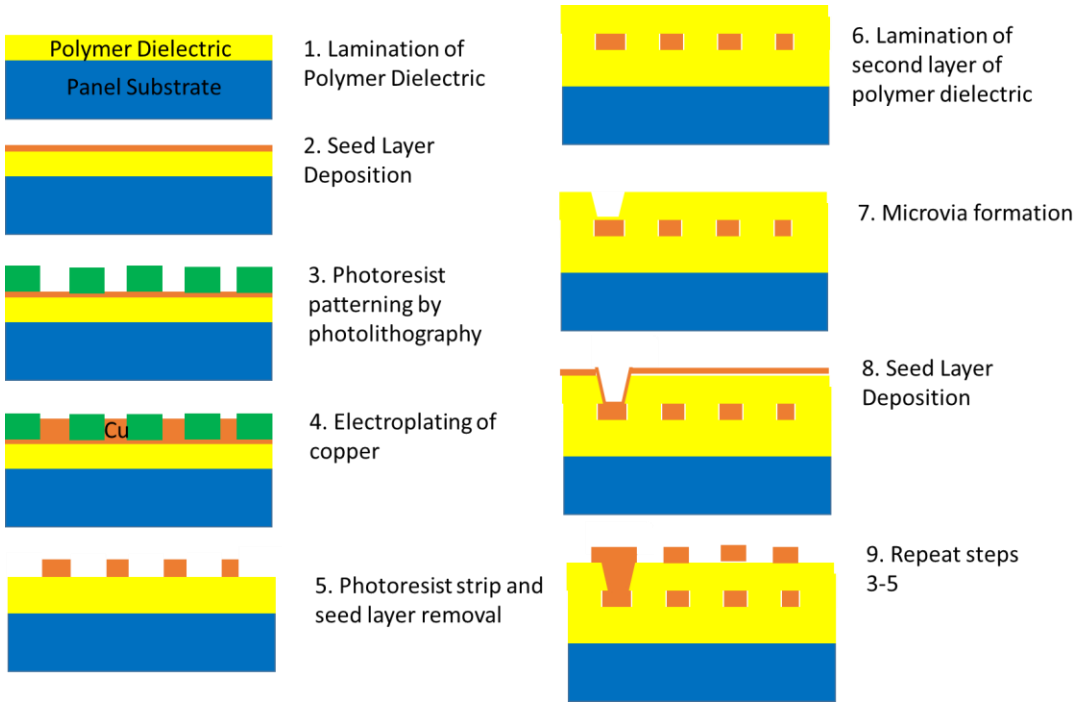


Figure 1-7: Summary of the current status of properties of polymer dielectrics [13]

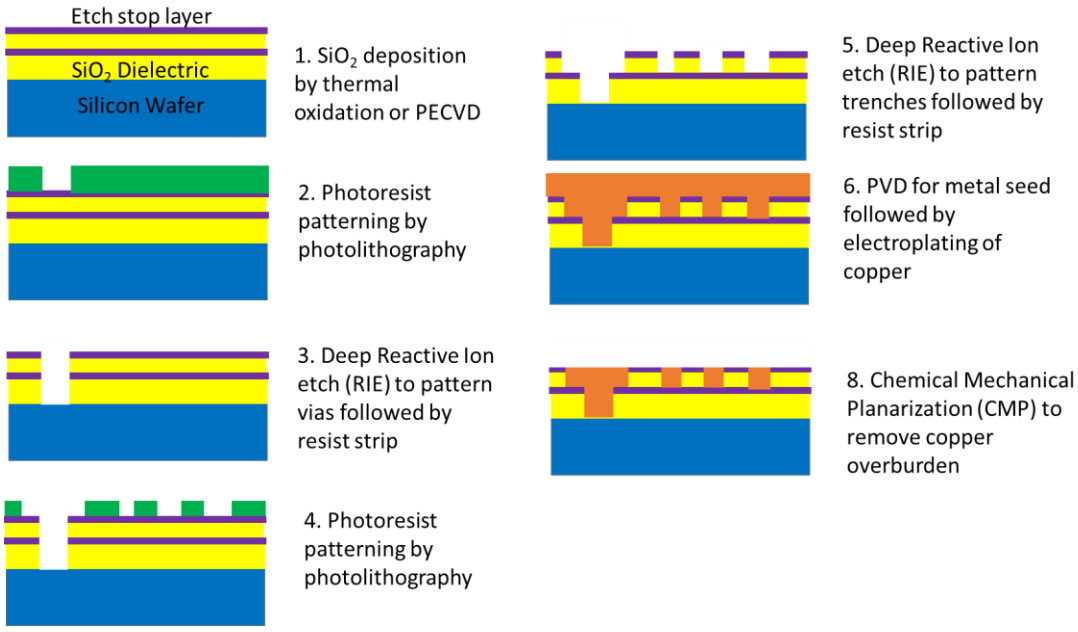
1.2.4 Processes

The current panel-based RDL utilizes a semi-additive process (SAP) to fabricate < 10 µm RDL. For wafer processes, back-end-of-line (BEOL) RDL is used to fabricate < 2 µm RDL. The process flows for SAP and BEOL RDL are summarized in Figure 1-8. Polymer-based SAP RDL suffer from fabrication challenges for fine width (< 3 µm) copper lines with seed layer removal process and the problem worsens as high aspect ratio lines are fabricated. Microvia scaling below 10 µm diameter is another concern for polymer RDL. There have been research efforts based on embedded trench RDL to overcome the seed layer etch challenge. However, embedded trench RDL requires dielectric patterning instead of photoresists as in SAP RDL. As discussed in the materials section, polymer dielectrics are permanent materials with the ideal set of electrical,

mechanical, thermal and chemical properties. Thus, the material design becomes challenging for patterning dielectrics with high resolution below 5 µm dimensions. As opposed to this, SAP RDL requires photoresist patterning which can be scaled down to nanometer dimensions as shown in transistor fabrication. The photoresist is a temporary material which is removed later and hence, material design is focused primarily on high resolution lithography. With SAP RDL, seed layer etch process is the primary challenge. The proposed research demonstrates, for the first time, a novel zero side-etch process to remove the seed layer and fabricate high aspect ratio < 5 µm copper lines and below. The proposed research also demonstrates a novel process to scale microvias in polymer dielectrics to 2 µm diameter and below.



(A)



(B)

Figure 1-8: Process Flows for: (A) SAP with Polymer RDL (B) Inorganic BEOL RDL

1.2.5 Reliability of 2 µm multi-layer RDL

The reliability of multi-layer polymer-based RDL is primarily focused on two aspects: (A) Line reliability, and (B) Microvia reliability. The electrical leakage failures between fine pitch RDL wiring (< 4 µm line and 4 µm space) due to electrochemical migration of copper in polymer dielectrics have limited the scaling down of polymer dielectric RDL to below 5 µm. Inorganic barriers like silicon nitride have been proposed in the literature to prevent copper migration [8]. However, since these are high D_k dielectrics (> 7) with ~ 200 nm thickness, the benefit of low D_k polymer RDL for high bandwidth system gets nullified. Further, the novel polymer dielectrics developed recently are halogen free materials (< 20 ppm of chlorine content). The moisture absorption of polymer dielectrics is becoming a critical factor for scaling down to 2 µm RDL. This research proposes to predict the rate of copper diffusion in such advanced polymer dielectrics with

varying levels of moisture absorption. For microvia reliability, the high degree of mismatch in the CTEs of glass (7.8 ppm/K), polymer dielectric (30-60 ppm/K) and copper (17 ppm/K) is a challenge when subjected to stresses in thermal cycle testing (TCT), an industry-standard reliability test. Reliability of 8-10 µm diameter microvias have been well established with polymer RDL [[6], [14]]. Finite element modeling (FEM) will be performed to characterize the stresses during TCT and predict the ideal CTE and modulus of polymer dielectric to achieve reliable 2 µm microvia interconnection.

1.3 Novelty of Proposed Research

This research addresses the limitations of the current state-of-the-art polymer RDL technologies by;

(A) Modeling and predicting the fundamental limit of laminate versus glass panel core materials for the minimum capture pad size required to land a microvia

(B) Electrical design of 2 µm panel-based polymer RDL for higher bandwidth (5X) and lower RC delay than silicon RDL

(C) Novel materials for reliable 2 µm RDL fabrication. Development of reliability models for 2 µm RDL structures will help predict the ideal set of elastic moduli, CTE, % elongation to failure and interfacial adhesion required. Novel dielectric materials will be developed with the help of these results.

(D) Advanced processes for 2 µm RDL fabrication including a novel zero-side etch seed layer removal process to fabricate high aspect ratio copper lines and novel process to scale microvia diameters to 2 µm and below.

(E) Reliability of electrochemical migration of copper lines with varying moisture absorption polymer dielectrics will be evaluated. The maximum tolerable moisture absorption of the polymer dielectric required to scale polymer based RDL to 2 μm and below will be predicted. Thermal cycling reliability of 2 μm microvia structures will be demonstrated with the material chosen with the predicted right set of properties as mentioned in (C).

A summary of the proposed research with key RDL technologies is summarized in Table 1-2. The term 'I/O wiring density' refers to the number of RDL wiring connections that can be made from one die to the other and is normalized to the edge length of die (in mm) and one layer of RDL. The key innovations of the proposed 2 μm RDL are summarized in Figure 1-9.

Table 1-2: Proposed RDL Vs. Current RDL technologies – Modeling, Design, Materials, Processes and Reliability

	Parameters	BEOL RDL (300 mm wafer)	Current RDL (500 mm panels)	Proposed Glass RDL
Modeling for layer-to-layer registration	Microvia Diameter/ Capture Pad	1-2/3-4 µm [6]	10 µm/ 25 µm [3]	2 µm/ 5 µm
Design for 2 µm RDL*	Data rate per signal line	2 Gbps	2-5 Gbps	> 10 Gbps
	Single Ended Impedance (Z_0 in Ω)	50	50	50
Materials (Ultra-Thin Dielectric Materials)	Material	SiO_2	Epoxy, Polyimide	Advanced Epoxy, Parylene
	Thickness	1-1.5 µm	6-8 µm	1.5-3 µm
	Dielectric Constant (At 1 GHz)	4.0	3.1-3.5 [[4],[6]]	2.3-3.1
	Young's Modulus	80 GPa	2-7 GPa	2-7 GPa
	% Elongation to Break	-	2-50 %	10-50 %
	Coefficient of Thermal Expansion (CTE)	0.6 ppm/K	35-55 pm/K	35 ppm/K
	Moisture Absorption (wt.%)	< 0.1 wt.%	> 0.5 wt.%	< 0.2 wt.%
	Adhesion to Copper	Excellent	Excellent	Excellent
Processes	Line Width/Spacing	1-2/1-2 µm	6/6 µm [4]	2/2 µm
	Microvia Diameter	1-2 µm	10 µm [3]	2 µm
	I/O wiring density in terms of IOs/mm/layer	> 200	50	> 200
Reliability of Multi-Layer RDL	Electrical Leakage failures between lines	Passes 1-2 µm RDL	Fails < 4 µm RDL [8]	Passes 2 µm RDL
	Microvia Reliability	Passes 1-2 µm RDL	Passes 10 µm RDL	Passes 2 µm RDL

(* Stripline assumed with 6 mm line length)

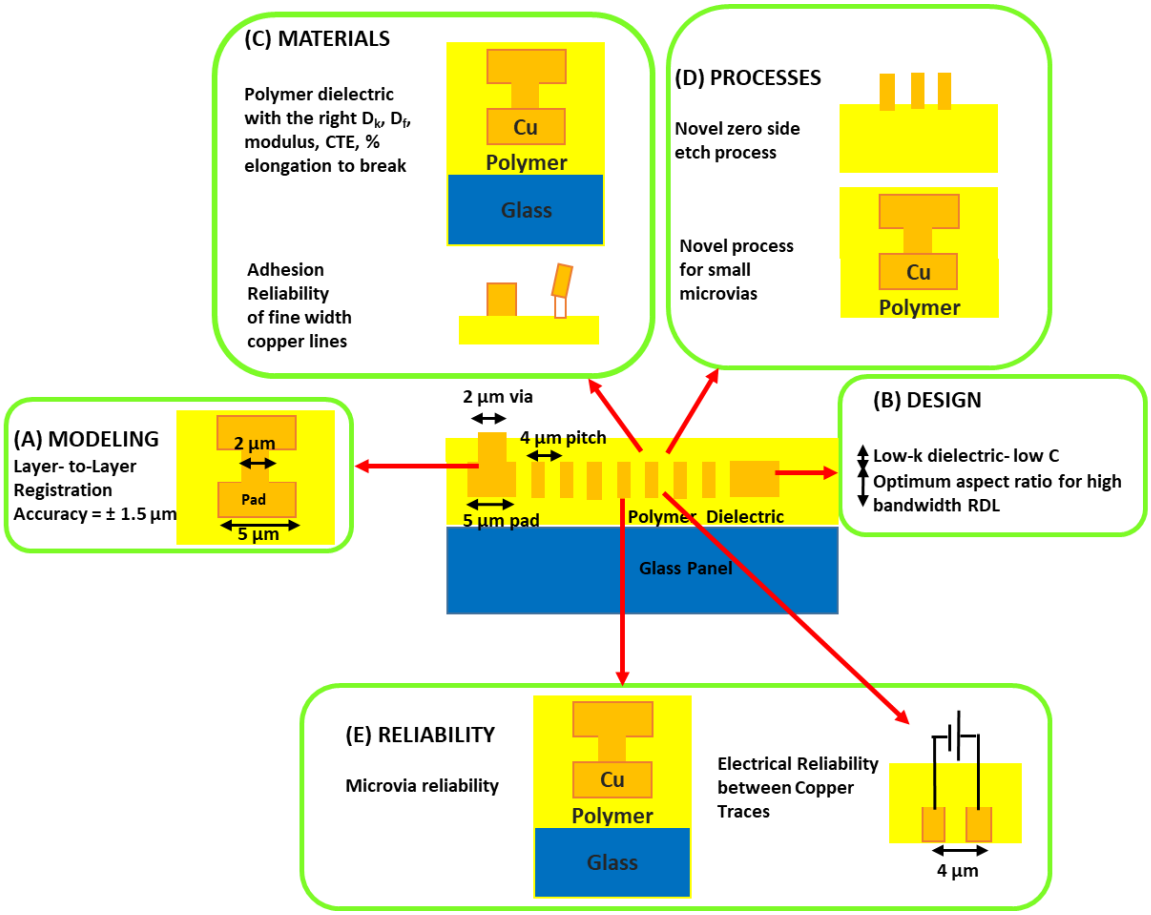


Figure 1-9: Key innovations of the proposed 2 µm multi-layer RDL stack-up for 2.5D glass panel

1.4 Research Objectives, Challenges and Tasks

The research challenges and tasks associated with the objectives are briefly summarized in Table 1-3.

Table 1-3: Summary of research objectives, challenges, and tasks

No.	Objectives	Challenges	Tasks
1	Model for layer-to-layer registration	Predict fundamental limit of capture pad size required to land a microvia for glass and organic laminate panels	Fabricate and characterize layer-to-layer dimensional shifts for glass and different modulus and T_g organic laminate panels
2	Design	Design 2 µm RDL with optimum aspect ratios of copper lines for high bandwidth, low RC delay with 50 ohms impedance matching	Propose Multi-Layer RDL stack-up with required conductor line and dielectric thicknesses
3	Materials	Novel, ultra-thin dielectric materials with the required electrical, mechanical, thermal and chemical properties	• Material with the right D_k, modulus, % elongation to break, CTE for reliable 2 µm RDL • Excellent interfacial adhesion to copper
4	Processes	• High aspect ratio copper lines • Scaling of microvia diameters to 2 µm and below	• Novel seed layer etch process to fabricate high aspect ratio lines with zero side etch • Novel process to demonstrate microvias with diameters 2 µm and below
5	Reliability of 2 µm multi-layer RDL on glass core	• Copper diffusion between fine pitch copper traces with polymer dielectrics • CTE mismatch between glass, polymer and copper	• Develop a model to predict the maximum tolerable moisture absorption with advanced polymer dielectrics • Modeling for different CTE and modulus of polymer dielectrics to predict microvia failures during thermal cycling reliability tests

1.5 Thesis Outline

Chapter 1 defines the background and motivation for the research, summarized state-of the art RDL technologies with their limitations, proposed novel approach to address these limitations, research challenges and tasks to achieve the desired research objectives.

Chapter 2 includes a critical literature review of the relevant prior work to address the fundamental challenges defined in Chapter 1.

Chapter 3 describes the modeling for layer-to-layer registration comparing state-of-the-art laminate core materials versus low CTE (3.3 ppm/K) and high CTE (7.8 ppm/K) glass panels. The laminate core materials are characterized for elastic moduli and CTE versus temperature. The core materials are characterized as it is without any polymer dielectric or copper RDL structures for dimensional shifts with heat and cool solder reflow cycles. Finite element modeling (FEM) is used to predict the dimensional shifts of the core due to varying percentage areas of copper patterns in the RDL structure. These models are experimentally validated using a two-layer RDL structure. The summation of dimensional shifts of the core with and without polymer dielectric and copper RDL structures is used to predict the minimum capture pad size required for landing a microvia.

Chapter 4 presents the electrical design simulations for high bandwidth, low RC delay, single-ended 50 ohms impedance matched RDL. In the first part, 2 µm line and 2 µm space RDL design is fixed and simulated with fixed dielectric thicknesses of 1 µm for stripline configuration comparing SiO_2 ($D_k \sim 3.9$, $D_f \sim 0.002$) and low D_k polymer dielectric parylene ($D_k \sim 2.3$, $D_f \sim 0.003$) for maximum signal efficiency. The maximum product of eye height and eye width is taken as the most efficient RDL structure in terms of signal integrity. The eye heights and eye widths are simulated for varying aspect ratios against frequencies/signal data rates for determining the improvement in bandwidth performance of polymer RDL versus silicon BEOL RDL. In the second part, the signal data rate is

fixed at 10 Gbps and the pitch of the RDL is fixed at 4 µm to maintain the exact I/O density as that for 2 µm line and 2 µm space structure. This design is simulated for varying line widths, line spaces, aspect ratios and dielectric thicknesses to determine the most efficient RDL structure in terms of signal integrity. This study is done for both stripline and embedded microstrip transmission line structures. Thus, the optimum polymer RDL structure is determined for high bandwidth 2.5D glass panel interposer.

Chapter 5 describes advanced materials for reliable 2 µm polymer RDL structure. Finite element modeling is used to simulate three-layer stacked microvia reliability (< 5 µm diameter). The model predicts the stress and strain in copper vias and polymer dielectrics for varying taper angles (55^0-90^0) and aspect ratios of (0.5-1.5), typically observed during fabrication of < 5 µm diameter microvias with ultra-thin polymer dielectrics. The Von Mises total mechanical strain values in copper vias at -55 °C and + 125 °C will help predict the number of cycles to failure using fatigue models. The Von Mises equivalent stress and total mechanical strain in polymer dielectrics will help predict the ideal CTE, % elongation to break, modulus and tensile strength of polymer dielectric required to pass microvia reliability without any cracks. The model will also include 2 µm copper line structures to predict the interfacial stress observed during thermal cycling. The interfacial stress will help predict the peel strength required for reliability of metal-polymer interface. The impact of different functional groups in polymer dielectrics on peel strength of metal-polymer interface will enable the design of novel low-k, non-polar polymer dielectric for enhanced interfacial adhesion.

Chapter 6 describes novel processes to scale polymer RDL to 2 µm and below. The research identifies the future need to scale RDL beyond 2 µm. The novel zero-side etch seed layer removal process will be demonstrated to enable fine pitch RDL. Microvia scaling is limited by polymer dielectric patterning as described in section 1.2.4. A novel process to scale microvia diameters below 2 µm will be demonstrated.

Chapter 7 presents reliability evaluation of fine pitch copper line RDL with varying moisture absorption polymer dielectrics. Layer-to-layer electrochemical migration of copper is evaluated using an advanced epoxy polymer dielectric with varying voltage and relative humidity levels. An RDL structure is fabricated with 2 µm line and 2 µm space using the same polymer dielectric to evaluate electrochemical migration reliability. Different polymer dielectrics with varying moisture absorption are evaluated for layer-to-layer electrochemical migration to predict the effect of moisture absorption. This chapter also includes demonstration of thermal cycling reliability of < 5 µm diameter microvias using the optimized material chosen from the results of chapter 5.

Chapter 8 describes summary and contributions of this dissertation.

CHAPTER 2. LITERATURE REVIEW

This chapter reviews the relevant published literature and recent prior art in addressing the fundamental challenges in modeling for layer-to-layer registration, design, materials, processes and reliability of fine pitch RDL.

2.1 Layer-to-Layer Registration with organic laminate panels

The layer-to-layer registration study is significant for determining the minimum capture pad required to land a microvia. The I/O density of RDL wiring is highly dependent on the size of the capture pad required as shown in Figure 1-5 and Table 1-1. The I/O wiring density of RDL decreases from ~ 235 to ~ 135 IOs/mm/layer with the capture pad size increasing from 5 µm to 25 µm. This leads to the decrement in the number of 2 µm width copper lines being routed from n=11 to n=6, which is a 45 % reduction in number of copper lines being routed. Thus, I/O wiring densities cannot scale to > 200 IOs/mm/layer with larger capture pads even if SAP RDL technology can achieve 2 µm line width and space. This implies the need to study the dimensional shifts in panel-based organic laminate and glass core materials in order to predict the fundamental limit of minimum capture pad required to land a microvia. The schematic showing the movement of capture pads during RDL processes is shown in Figure 2-1.

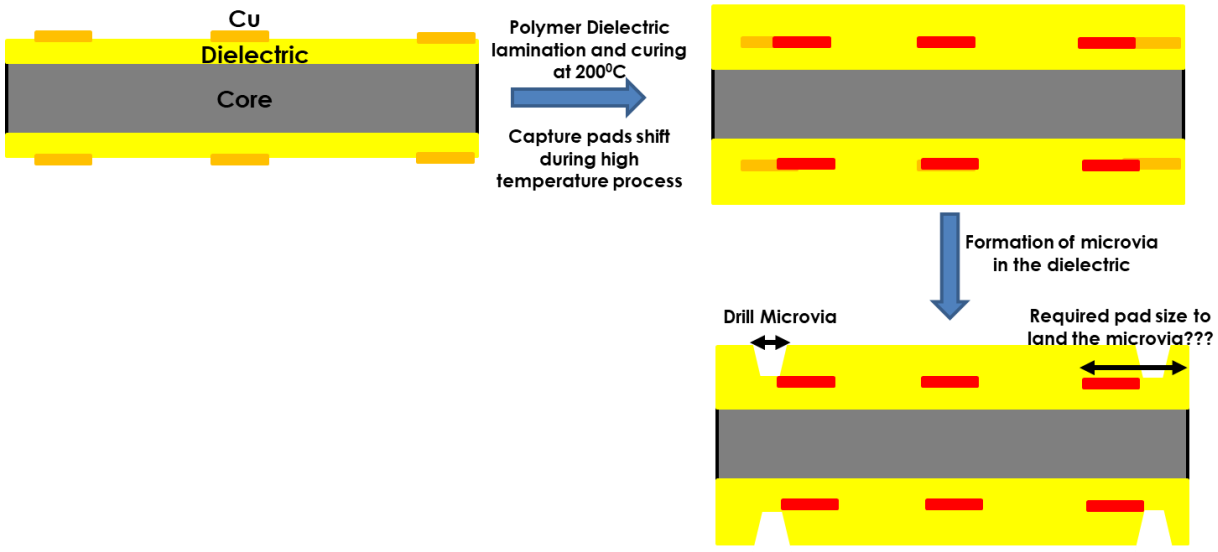


Figure 2-1: Schematic showing the movement of capture pads during RDL processes

Currently, BEOL RDL with a total of 4-5 metal layers of 1 µm thickness each is fabricated using a 775 µm thick silicon core. Thus, BEOL RDL faces minimum dimensional shifts since the copper metal layers are thin and the high elastic modulus of silicon (~ 110-120 GPa) comparable to electroplated copper (~110 GPa) makes it dimensionally stable to thermal excursions. The organic laminate core currently used with SAP RDL is 100-1000 µm thick. However, the low elastic modulus of laminate (10-20 GPa) core causes dimensional shifts with thick copper layer processing. Today, most studies have employed compensation-based strategy to solve this issue with limited success. For most of these approaches, assuming a large 500 mm x 500 mm panel, a layer of the original RDL design is fabricated on a dummy substrate and the co-ordinates of alignment marks are tracked before and after the thermal excursion process. Thousands of such dummy substrates are fabricated to understand dimensional shifts from one metal layer to the next metal layer. The mask designs for capture pads are compensated based on these measurements [[15], [16], [17]]. Attila et al. reported the shrinkage is primarily isotropic for a PCB laminate core like FR-4 as shown in Figure 2-2 and showed that it can be predicted through a linear equation

[15]. With a new stencil compensation technique, the registration shifts were reduced from (-100 to +140 µm) to (-30 to +80 µm) as shown in Figure 2-3. The laminate core used in the study is a PCB grade material and not commonly used for fine pitch, package substrate RDL. Laminate cores with different CTEs, elastic moduli and glass transition temperatures (T_g) need to be evaluated to study the optimized registration shifts during RDL processing. Also, such compensation strategies are ideal for large area mask-aligner based contact lithography which is not fit for fine pitch RDL due to non-availability of auto-alignment function, contamination of expensive glass masks with photoresists during photolithography exposures. Projection steppers are used for fine pitch RDL photolithography (< 5 µm) and the auto-scaling function in such stepper tools can compensate upto 0.05-0.1 % isotropic expansion or shrinkage using demagnification or magnification of UV beam during exposure [18]. This is shown in Figure 2-4. The projection steppers work on the principle of step-by-step UV exposure shots with each step size being fixed. For example, if the maximum shot size of a projection stepper tool is 100 mm x 100 mm, it will require 25 shots to expose the entire panel of size 500 mm x 500 mm. Hence, mask compensation strategy does not work for projection steppers since each exposure shot will require a separate compensated mask, turning out to be a super expensive process. Assuming a median value of 0.075% compensation for a single 100 mm x 100 mm exposure shot area, the UV beam can be magnified or de-magnified by a total of 75 µm. This translates to a tolerance level of ~ 37 µm for shift in copper capture pad structure that can be auto-compensated by the projection stepper tool. Any shift above this tolerance level cannot be auto-compensated and will lead to excessive capture pad being required. For example, a capture pad shift of 50 µm for 100 mm length in one direction (500 ppm) during thermal processing will lead to a minimum capture pad size of ~ 13 µm plus the diameter of microvia required to land the microvia. Thus, the common strategy today is to use a smaller

exposure shot like 20 mm x 20 mm, where for the similar 500 ppm shrinkage, the capture pad shift will be of the order of 10 µm. With 0.075% auto-scaling function, a shift of 7.5 µm is auto-compensated and hence, the minimum capture pad size required to land the microvia will be 3 µm plus the diameter of microvia. This strategy, being used currently with organic laminate panel substrates for smaller capture pad diameters, decreases the throughput of photolithography to a large extent. With 20 mm x 20 mm exposure shot size, it will require 625 shots to expose the entire panel of size 500 mm x 500 mm.

Products	Size (mm × mm)	Pre-preg	Manufacturer
PA	335 × 240	S-1000	M1/M2

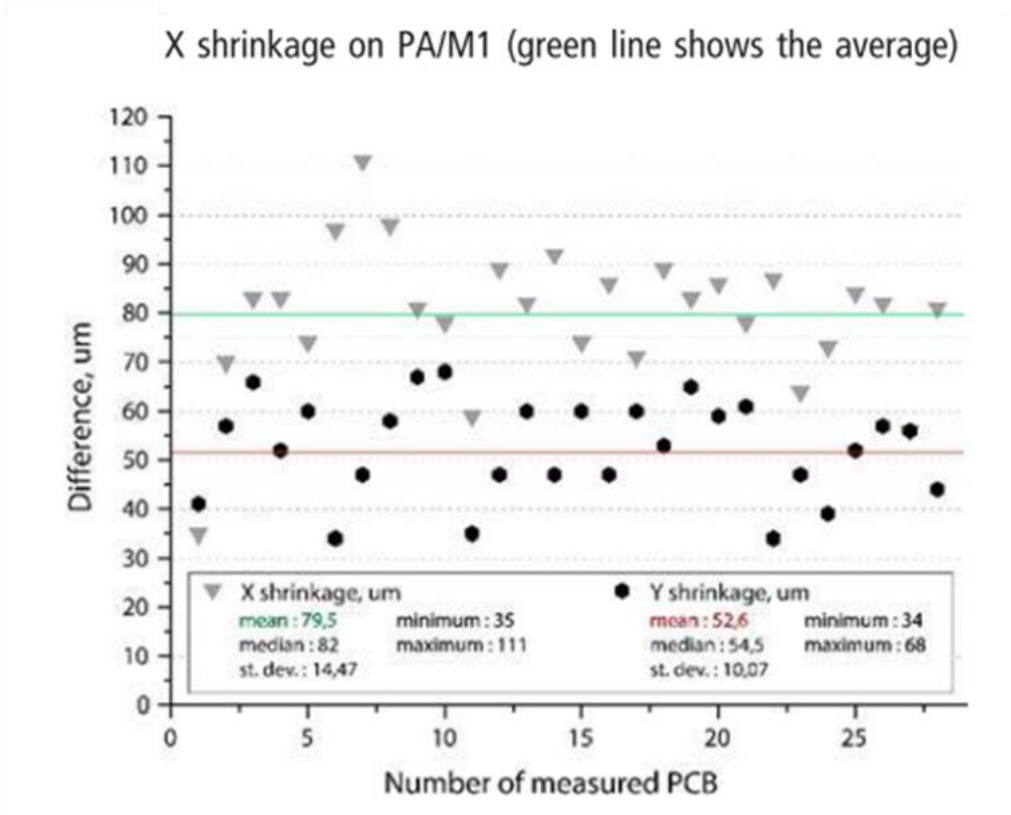


Figure 2-2: X and Y shrinkage for a PCB laminate core revealing highly isotropic nature of shrinkage (X-direction shrinkage ~ 238 ppm and Y-direction shrinkage ~ 219 ppm) [15]

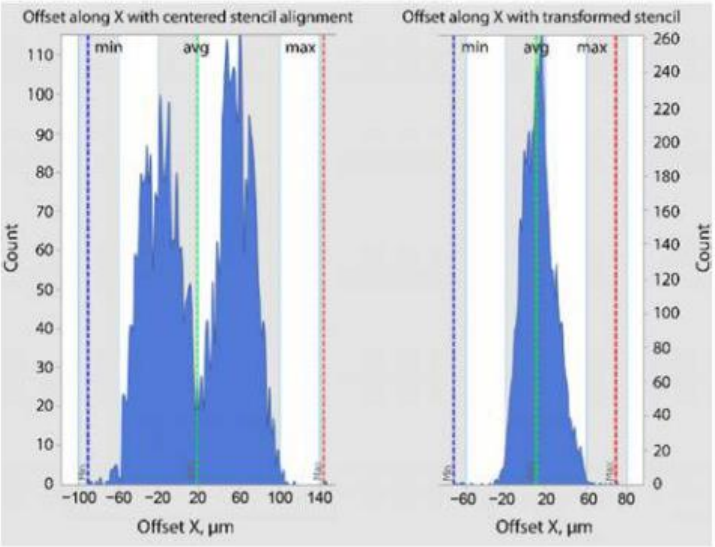


Figure 2-3: Improved compensation technique showing decrement in X- shrinkage [15]

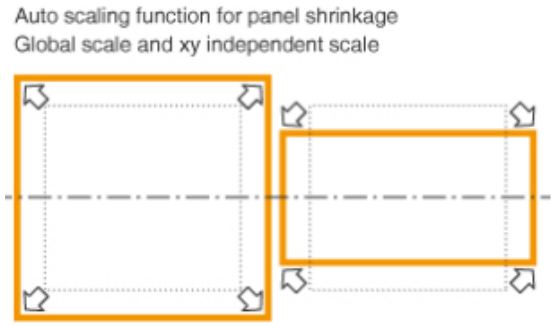


Figure 2-4: Auto-scaling function for panel shrinkage in advanced packaging stepper tools [18]

Alexandra et al. reported that the organic laminate FR-4 core is manufactured at 180^{0}C and the material goes through an incomplete curing shrinkage and residual stress release during soldering reflow processes at 260 ^{0}C [16]. The residual stresses are developed during the cooling process after manufacturing at 180 ^{0}C due to the CTE mismatch between glass and resin present in the laminate core. These stresses are released during the first solder reflow cycle at a peak temperature of 260 ^{0}C. This was confirmed with thermo-mechanical analysis (TMA) studies studying shrinkage in Z-direction post two solder reflow cycles [16]. TMA studies with two solder

reflow cycles at a peak temperature of 260 ^{0}C confirmed that the post-curing process still induced some irreversible dimensional changes in laminate core during the second run. This is shown in Figure 2-5. The study was also performed with a sample being heat treated using a solder reflow cycle at a peak temperature of 260 ^{0}C and confirmed that the post curing shrinkage still induced similar amount of dimensional change in the laminate core as shown in Figure 2-6. There is no study on the effect of copper RDL patterning and the incomplete curing shrinkage behavior with different T_g and CTE laminate cores. The proposed research will consider the effect of: (A) Different T_g and CTE laminate cores along with low CTE (3 ppm/K) and high CTE (7.8 ppm/K) glass cores and, (B) Different percentages of copper RDL on layer to layer dimensional shifts.

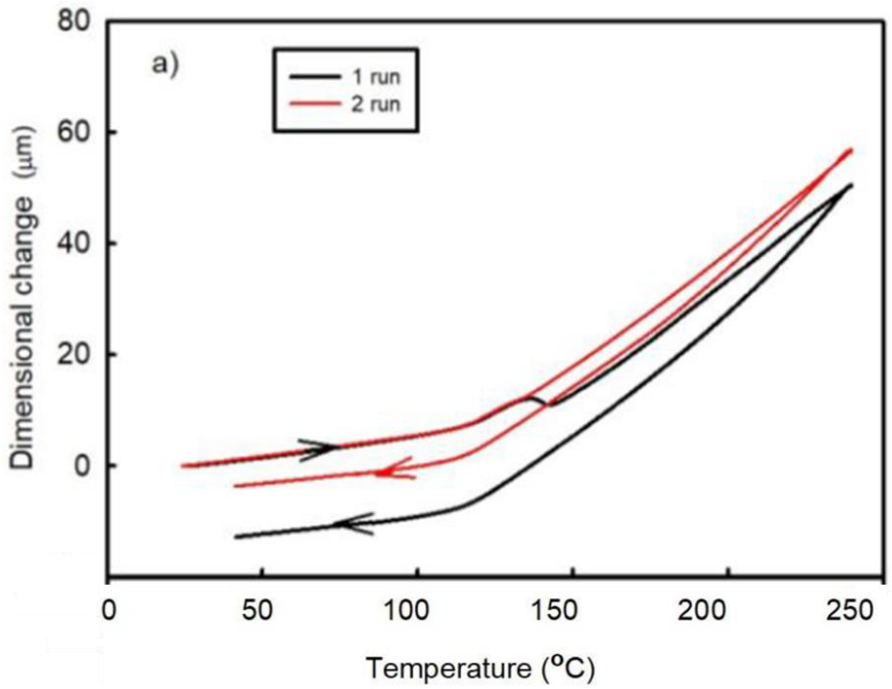


Figure 2-5: Dimensional change in Z-direction of FR-4 laminate core post one and two runs of solder reflow cycles at a peak temperature of 260 ^{0}C [16]

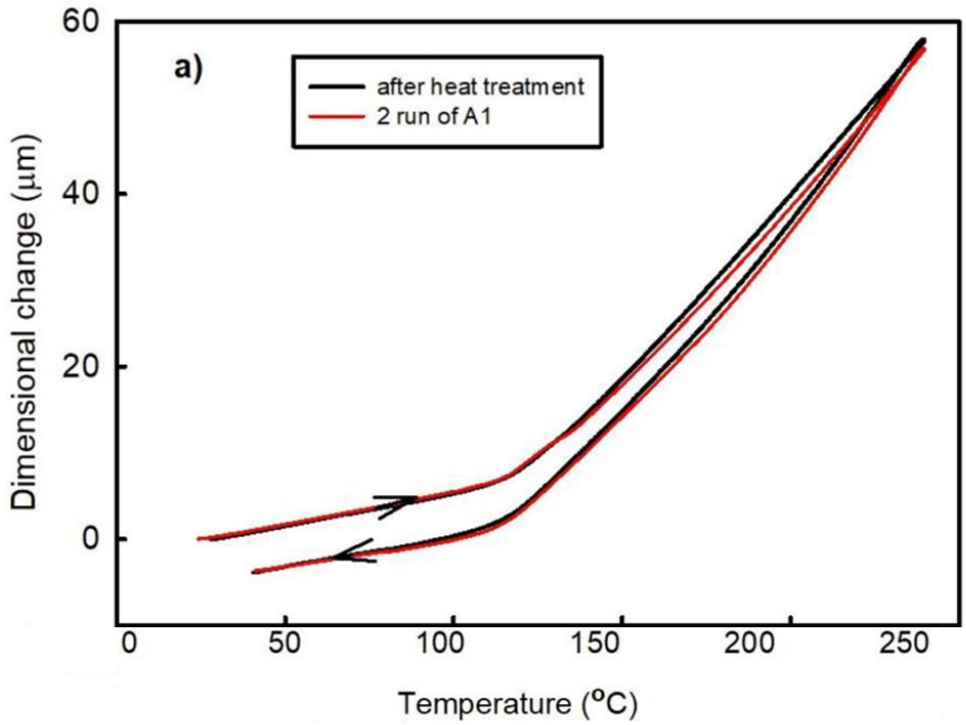


Figure 2-6: FR-4 laminate cores (named as A1 here) showing similar dimensional changes for the first TMA run of the heat treated sample using a solder reflow cycle of 260 ^{0}C and for the second TMA run of non-heat treated sample [16]

2.2 Design for multi-layer RDL with low RC delay

Andy Heinig compared RC parasitics for conventional polymer dielectric based SAP RDL versus inorganic SiO_2 BEOL RDL. The results were summarized in Figure 1-6 [11]. From the figure, the motivation to pursue polymer based RDL to reduce RC delay is clear.

The I/O density of the polymer RDL mentioned in Figure 1-6 is limited to < 50 IOs/mm/layer as compared to SiO_2 BEOL RDL with > 200 IOs/mm/layer. To overcome this reduction of I/O density in SAP RDL, one needs to have higher number of metal routing layers which in turn lead to high substrate costs due to low yields. This is highlighted in Figure 2-7. There are 24 signal rows to be routed and interconnected from a typical GPU die to a single HBM die stack architecture at 55 µm pitch [19]. Assuming a typical chip bump pitch at 40 µm with 24 rows

of signal bumps and pad diameter is 8 µm as shown in Figure 7, the polymer RDL at 10 µm L/S will route and interconnect only 2 rows of bumps in each metal layer, compared to 7 rows with SiO_2 BEOL RDL at 2 µm L/S. Thus, to complete interconnection of all 24 rows of GPU to HBM, polymer RDL with 10 µm L/S will require 12 metal layers compared to just 4 metal layers with SiO_2 BEOL RDL. This is the primary reason why 2.5D silicon interposer with SiO_2 BEOL RDL is in production for high performance computing package architectures. Thus, the primary objective is to develop a polymer RDL technology design, material and process system to achieve both: (A) High Bandwidth, low RC delay RDL to improve electrical performance and, (B) Very high I/O density RDL > 200 IOs/mm/layer to minimize the number of fabricated metal routing layers. This requires an optimum design by varying line widths and space at a fixed line pitch of 4 µm to maintain the required I/O density of > 200 IOs/mm/layer, using a dielectric material with lower dielectric constant and optimized dielectric and metal thicknesses. These parameters will optimize the design for low resistance, capacitance and crosstalk between the signal lines, enabling high bandwidth RDL with lower delay.

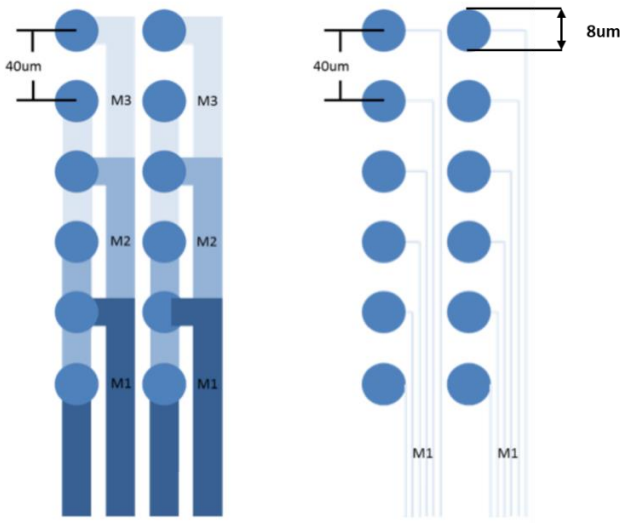


Figure 2-7: Polymer RDL requiring more metal routing layers compared to inorganic SiO2 BEOL RDL [11]

Kyungjun Cho et.al. studied in detail the signal integrity analysis of high bandwidth memory channels using a 2.5D silicon interposer system. There are two main types of transmission line structures used in interposer RDL: (A) Embedded microstrip line and (B) Stripline. This is shown in Figure 2-8. The research models highlighted in the paper identifies parameters like changing line width and space with silicon interposer BEOL RDL to understand the effect on insertion loss, far-end cross talk (FEXT) and near-end cross talk (NEXT). The dielectric thickness and metal thickness are kept constant at 1 µm, while the line width and space are interchanged between 2 and 3 µm. The research identifies the need for various repeater circuits and active circuits like equalizers for extending the signal data rate of silicon interposer BEOL RDL from 2 Gbps to 8 Gbps [20]. Figure 2-9 indicates how the eye is completely closed for silicon interposer BEOL RDL as the data rate increases from 2 Gbps to 8 Gbps without using any additional circuits.

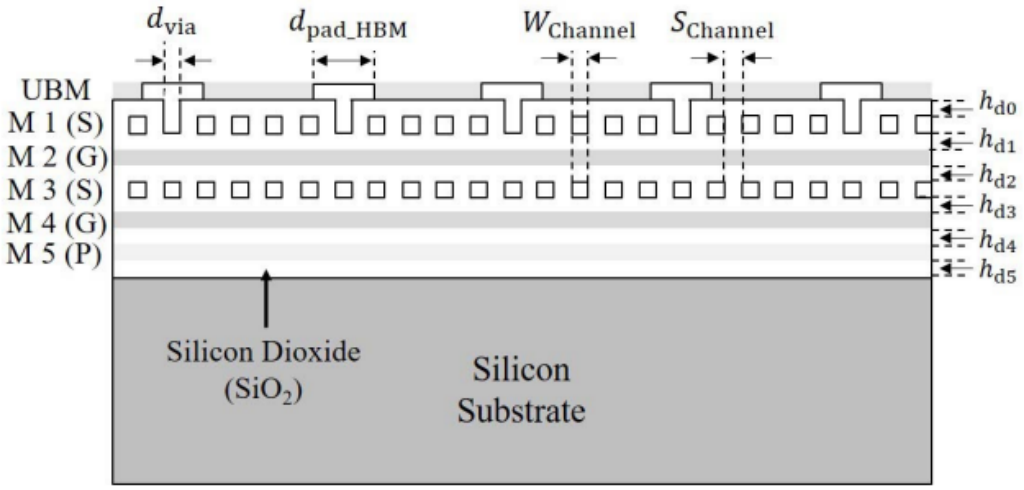


Figure 2-8: Embedded Micro-stripline and Stripline are used as signal channels for data transmission from High Bandwidth Memory (HBM) die to Graphical Processing Unit (GPU) die [20]

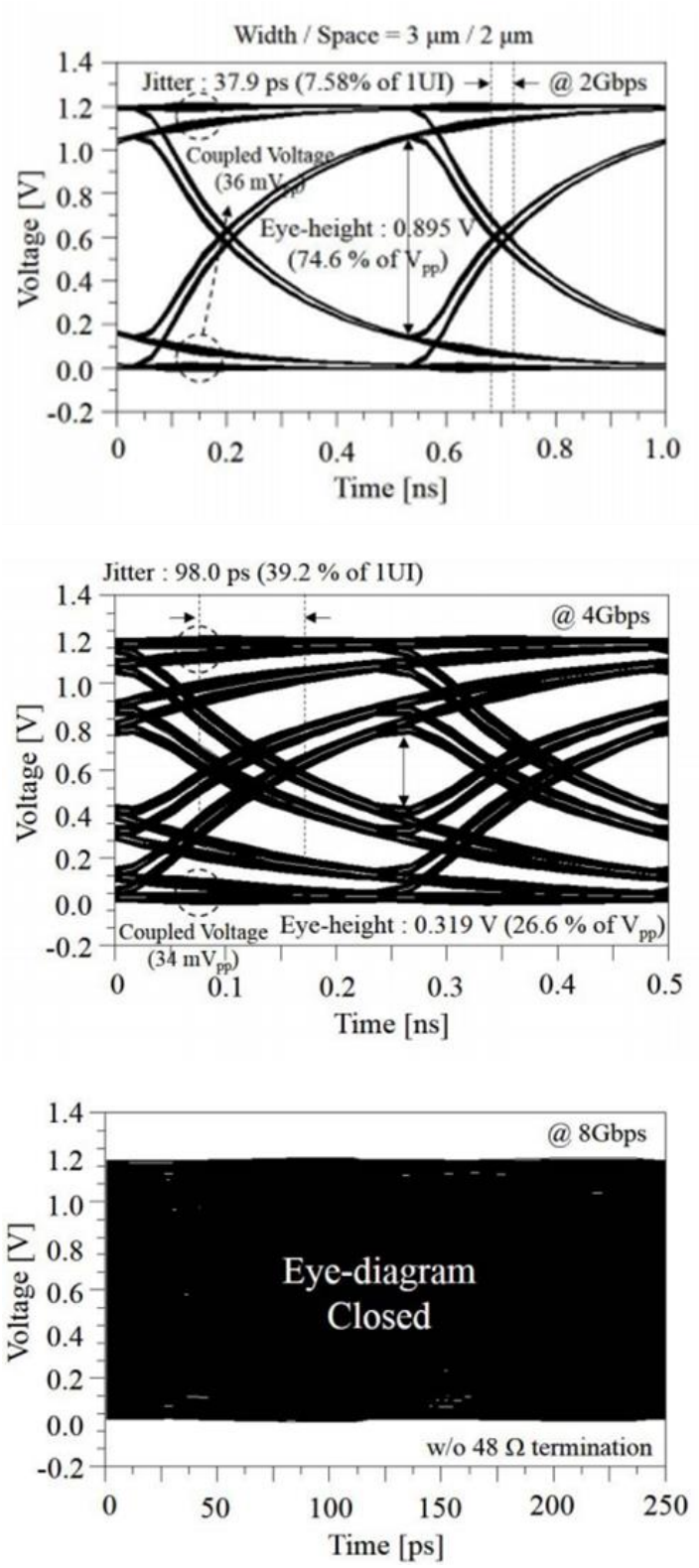


Figure 2-9: Eye diagrams for stripline configuration with 3 µm width and 2 µm space with increasing data rate for silicon interposer BEOL RDL [20]

Andrew Martwick et.al. highlighted the importance of equalization at the driver level while designing for optimum bandwidth performance of silicon BEOL RDL at 2 µm line and 2 µm space [21]. The capacitance of the interposer RDL is the biggest contributor at 1.6 pF for a typical 6 mm line length as shown in Figure 2-10 and equalization circuit is used to reduce the capacitance and increase the data rate per signal line from 2 Gbps to ~ 6 Gbps for 6 mm long line.

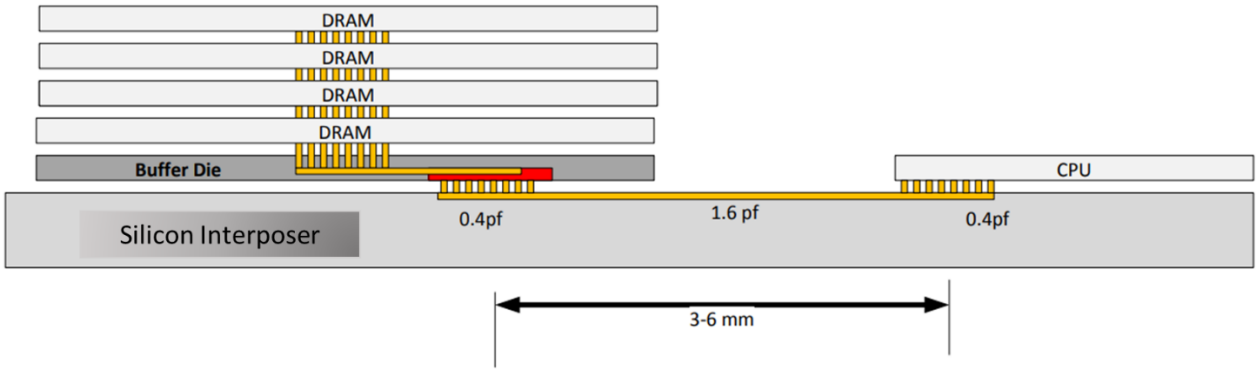


Figure 2-10: Interposer connection from HBM to GPU highlighting the biggest contributor to capacitance is RDL [21]

2.3 Materials for 2 µm Multi-layer RDL

The different RDL process technologies with their current capabilities are summarized in Table 1-1. The focus of this section is to introduce two main material technologies used in high density polymer RDL: (A) Photoresists for patterning of 2 µm line width and 2 µm space and, (B) Polymer dielectric with the required electrical, mechanical, thermal and chemical properties. Current photoresists used in package substrates are dry film negative-tone resists for direct lamination on large panels. The resolution of negative-tone photoresists in package substrates is still limited to 3 µm RDL with 7 to 15 µm thick resists [22]. Positive-tone spin-on resists for BEOL RDL can pattern 1-2 µm RDL and much below but usually at lower aspect ratios. The proposed research will utilize newly developed positive-tone chemically amplified dry film photoresists for

direct application on large panels. The use of chemically amplified photoresists addresses both the challenges of, high aspect ratio and fine resolution patterning, simultaneously.

Polymer dielectric material is the most significant component of RDL. The most common classes of polymer dielectrics that have been in use for the last three decades or so have been epoxy, polyimide (PI), benzocyclobutene (BCB), polybenzoxazole (PBO) and recently some fluoropolymers [[23], [24], [25], [26]]. The properties of these dielectrics have been summarized in Table 2-1.

Table 2-1. Comparison of polymer dielectrics

Parameters	Epoxy [23]	Polyimide (PI) [24]	Polybenzoxazole (PBO) [24]	Benzocyclobutene (BCB) [25]	Advanced Fluoropolymer [26]
Dielectric Constant (At 1 GHz)	3.1	3.2	2.9	2.65	2.6
Young's Modulus (GPa) (at 25 ^{0}C)	4	3.5	2.2	2.9	2.4
Tensile Strength (MPa) (at 25 ^{0}C)	93	200	170	87	100
% Elongation to Break	5	45	100	8	28
Coefficient of Thermal Expansion (CTE) (in ppm/K from 25-150 ^{0}C)	46	35	60	42	60
Moisture Absorption (wt.%)	1.1	1.1	1.5	< 0.2	< 0.4
Curing Temperature	180 ^{0}C/ 1 hour	350 ^{0}C/ 1 hour	200-250 ^{0}C/ 1 hour	250 ^{0}C/ 1 hour	190 ^{0}C/ 2 hours
Adhesion to Copper	Excellent	Excellent	Good	Poor	Poor

In general, epoxies are known for their low curing temperatures (< 200^0 C) and excellent adhesion to copper but suffer from limited microvia resolution. Polyimides have high % elongation to break like PBOs but suffer from high moisture absorption and high curing temperatures. PBOs additionally suffer from reliability failures at low temperatures [27]. Although the low dielectric constant of BCB is important for low RC delay RDL but it suffers from poor mechanical properties. Fluoropolymers have been recently developed as copolymers retaining the properties of epoxies, polyimides and BCBs. However, they still suffer from very high CTE (> 60 ppm/K).

These dielectrics need to meet the intrinsic and thermal stresses during fabrication of RDL with thick, high aspect ratio, fine pitch RDL. The same dielectric needs to be processable to pattern 2 μm diameter microvias as well. The research will try to identify the requirements of dielectric properties and demonstrate high aspect ratio RDL with the best identified dielectric material.

The material design of polymer dielectrics should consider two different aspects: (A) Reliability of stacked microvias and, (B) Interfacial adhesion of fine width copper lines (< 5 μm) on polymer dielectrics. In addition to this, the dielectric constant and dielectric loss tangent of the material should be as low as possible. The first aspect of designing for reliability of stacked microvias considers the CTE (thermal), tensile strength, elastic modulus and % elongation to break (mechanical) properties of the polymer dielectric. The second aspect of interfacial adhesion brings into the ideal chemical property required for the polymer dielectric. This covers the whole spectrum of properties of polymer dielectric required for material design research.

The first aspect of designing for reliability of stacked microvias will identify the required CTE, % elongation to break and modulus of polymer dielectric to pass thermal cycling reliability of 2 μm diameter microvias. There have been several modelling studies that have been

demonstrated to characterize the effects of aspect ratios, dielectric CTE, modulus and other important properties on the plastic strain failures of copper in microvias [[28], [29], [30], [31]. The diameters of the microvias in all these studies range from 5 µm to 75 µm. Saketh Mahalingam et.al. studied the effect of dielectric properties on the plastic strain in copper for > 50 µm microvia structures [30]. The total strain range (TSR) in copper while thermal cycling between -55^{0}C and +125^{0}C is used as a metric to predict fatigue failures in copper. The results are summarized in Figure 2-11. Fatigue models such as Engelmaiers' shown in equation (2-1) are used to predict the number of cycles to failure during thermal cycling based on TSR values in copper [14]. In equation (2-1), $\Delta\varepsilon$ is the total strain range (TSR), N_f is the number of cycles to failure, Df (=0.302) is the ductility coefficient of copper, R_m (=400 MPa) is the tensile strength of copper, and E_{Cu} (=117 GPa) is the Young's modulus of copper.

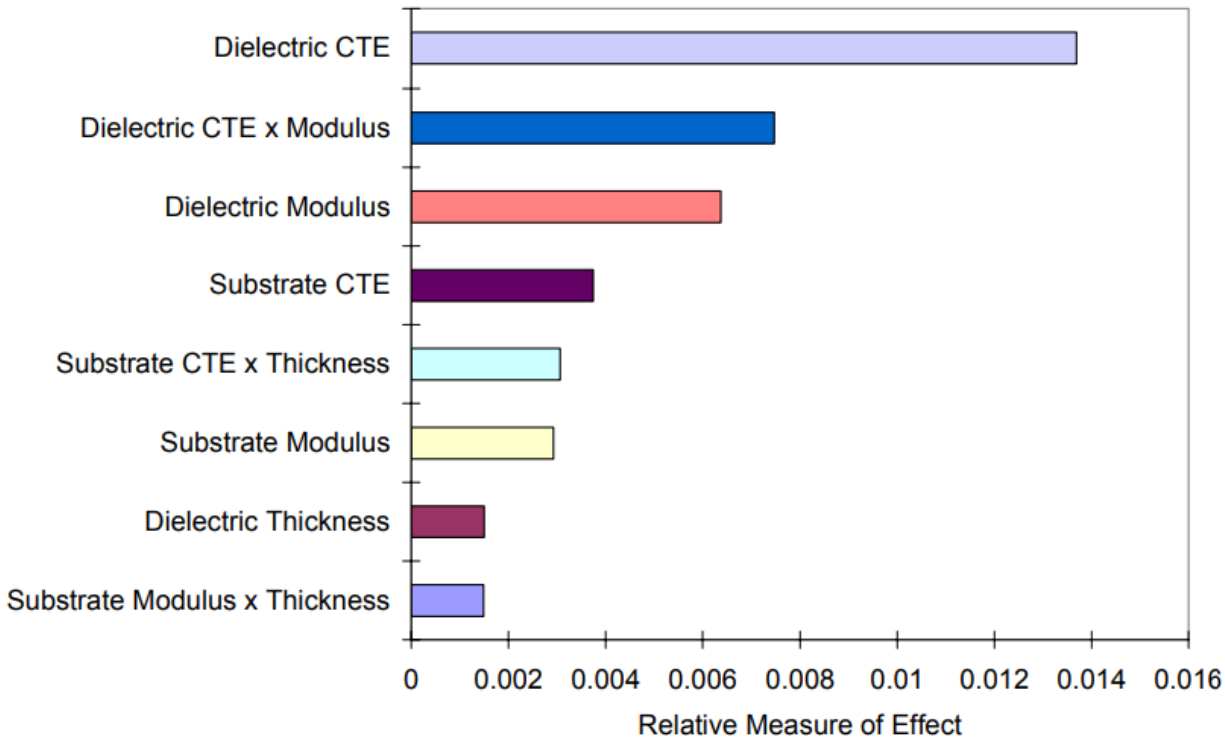


Figure 2-11: Effect of dielectric and substrate properties on microvia strain [30]

$$\Delta\varepsilon = N_f^{-0.6} D_f^{0.75} + 0.9 \frac{R_m}{E_{Cu}} \left(\frac{e^{D_f}}{0.36}\right)^{0.1785 \log\left(\frac{10^5}{N_f}\right)}$$

Eq. (2-1)

There have been several demonstrations of 3-10 µm diameter microvias in terms of patterning ability of dielectrics [[32], [33]]. However, the only demonstration of reliability is for 8-10 µm diameter microvias in 10 µm thick polymer dielectrics [[6], [14], [32]]. The aspect ratios of the microvias while shrinking to < 5 µm diameters with ultra-thin dielectrics have been well below 1 and hence, do not present major challenges in terms of reliability. However, the wall angle of the microvias have significantly decreased from the ideal 90^0 to 55-75^0 while shrinking microvias to < 10 µm [[7], [33]]. The reliability of these tapered microvias (< 5 µm diameter) with respect to strain in copper and stress and strain in polymer film have not been studied for different CTEs and moduli of polymer dielectrics. The strain in copper will help predict the total cycles to failure for microvia cracking in copper. The stress and strain values in polymer dielectric film will help predict if the polymer dielectric will crack during thermal cycling. This research will help identify the required mechanical and thermal properties of future polymer dielectrics for reliable small microvia formation.

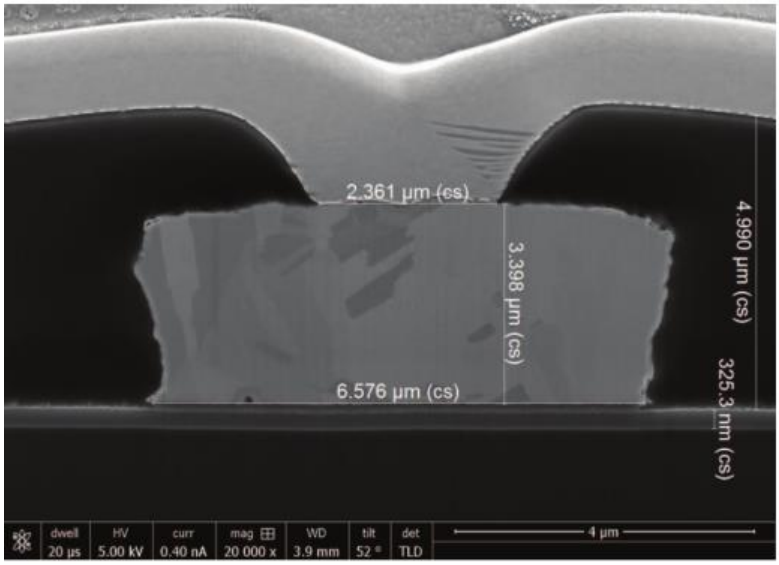


Figure 2-12: Tapered microvias (~ 63^0) below < 5 µm diameter [33]

The second aspect of material design is for enhanced adhesion between metal seed and polymer dielectric while scaling to fine pitch (< 5 µm) RDL. As fine pitch RDL scale for high signal data rate (higher frequency) transmission lines, polymer dielectrics need to be smooth for reliable processing. The most advanced dielectrics today have average surface roughness (R_a < 20 nm) and the average peak-to-valley roughness (R_z < 100 nm). Traditionally, electroless copper seed layer has been used for deposition of thin copper seed layers (~ 400-1000 nm thick) on to epoxy polymer dielectrics in panel-based laminate package substrates. The polymer dielectrics are roughened by a wet etch permanganate desmear process and the copper seed is deposited using a palladium activator catalyst. The copper seed is anchored to the polymer dielectric and results in excellent adhesion of copper metal to epoxy dielectrics. With the need for smooth interfaces, sputtered titanium and copper seed is deposited today using panel-based physical vapor deposition (PVD) tools. The interfacial adhesion between titanium seed and polymer dielectric has been characterized by peel strength tests and there has been no standard as to what the required peel strength is to fabricate 2 µm copper line RDL reliably. The proposed research tries to address this

challenge by characterization of interfacial stresses using finite element modeling during thermal cycling between -55^0C and $+125^0$C. The research will help predict the required peel strength between copper and polymer dielectrics as aspect ratios scale to > 1.

Tobias et al. used a simple relation shown below to predict the critical compressive stress for delamination of thin copper film from polymer dielectric [[34][35]].

$$\sigma_{critical} \text{ (in MPa)} \times \text{thickness of copper film (in } \mu\text{m)} \approx \text{Peel strength (in N/m)} \quad \text{Eq (2-2)}$$

This relation has been validated by Tobias et al. to predict delamination failures due to compressive stresses in copper film at copper-polymer interfaces.

2.4 Processes for 2 µm Multi-layer RDL

As noted in the introduction section, there are two main RDL technologies that are in production today: (A) BEOL process mainly used for 300 mm wafer platform, and (B) SAP RDL for both 300 mm wafer and 500 mm panel platforms. A process flow of these RDL technologies is shown in Figure 1-8. The cross-sectional view of a BEOL RDL structure as used for production in high density 2.5D embedded fan-out package substrate is shown in Figure 2-13 [36].

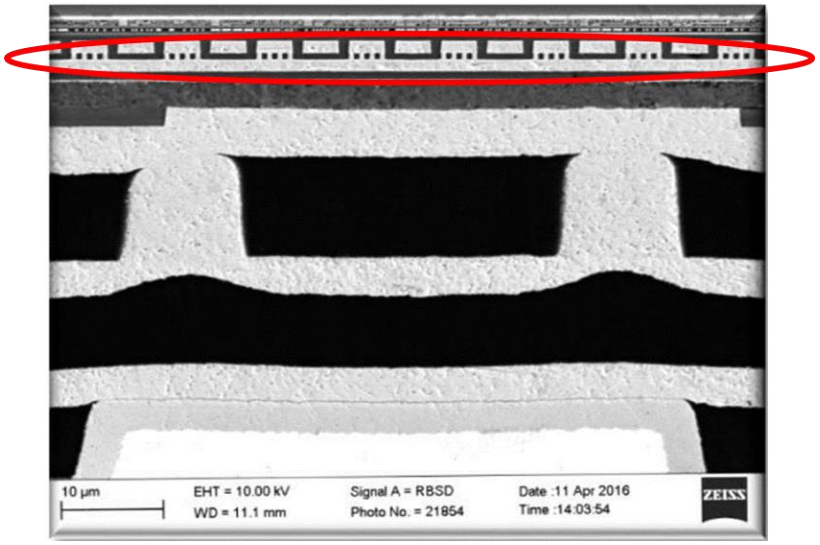


Figure 2-13: Cross sectional view of Hybrid BEOL + Polymer RDL stack used for high volume production in high density embedded fan-out with BEOL RDL showing ~ 3 µm line width and ~ 1 µm space [36]

There are four critical steps in fabrication of 2 µm polymer dielectric RDL: (A) Photolithography for 2 µm line width and 2 µm space, (B) Seed Layer Etching, (C) Planarization, (D) 2 µm diameter microvia formation. The issue of photolithography is addressed by novel photoresist materials as discussed in section 2.3. There have been demonstrations of 2 µm polymer RDL at aspect ratio of 1 using liquid spin-on processes on wafers [[5], [36], [37]].

Seed layer etching is another big challenge in the formation of fine pitch copper traces. Copper seed layer removal is still a wet isotropic etching process. One of the strategies package substrate companies are adopting is to reduce dielectric roughness with reliable adhesion of copper seed to polymer dielectrics [38]. The concept is shown in Figure 2-14, which highlights the theoretical estimation of critical dimension (CD) loss of the line width due to side-etch during the seed layer removal process. The other strategy is to compensate the design mask for side-etch and use thin seed layers with thickness bare enough to plate an entire wafer or panel uniformly [39].

The copper layer patterns are electroplated on to a dummy substrate and etched under optimized conditions using an end-point detection step. Once the seed layer is removed, the widths of copper patterns are measured, and the design is compensated. For example, to enable fabrication of 3 µm line width and 3 µm space and if the side-etch measured is 1 µm, the mask design is compensated to 4 µm line width and 2 µm space. However, this strategy is not scalable since for 2 µm line width and 2 µm space, it is very difficult to pattern resists with 3 µm width and 1 µm space. The problem becomes even more difficult to overcome when scaled to 1 µm line width and 1 µm space. Also, since copper seed etching is a diffusion limited process, the seed removal of high aspect ratio copper traces is a bigger challenge [39]. The seed layer is usually over-etched to 150-200 % of seed layer thickness to ensure complete removal of seed layer across the wafer or panel substrate [39]. A study was performed to calculate the measured and theoretical CD loss of 2 µm line and 2 µm space RDL with an aspect ratio of 1.5 for 150% seed over-etch by varying copper seed thicknesses as shown in Figure 2-15 [39]. The improvement is due to advances in seed layer etch chemistries targeting differential etching of small grain copper seed compared to large grains of electroplated copper [40]. Thus, for a typical 150-200 nm thick sputtered seed layer in polymer RDL, the CD loss ranges between 0.4-0.6 µm. The CD loss will be more prominent as polymer RDL scales to 1 µm line width and 1 µm space RDL. This research proposes to develop a novel zero side-etch process to scale package substrate RDL to 1-2 µm RDL and below.

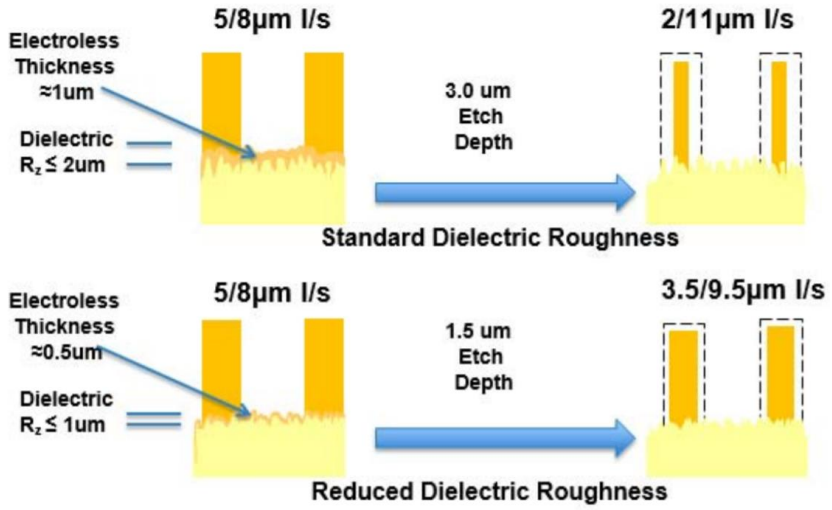


Figure 2-14: Schematic showing narrowing of copper traces after seed layer removal [38]

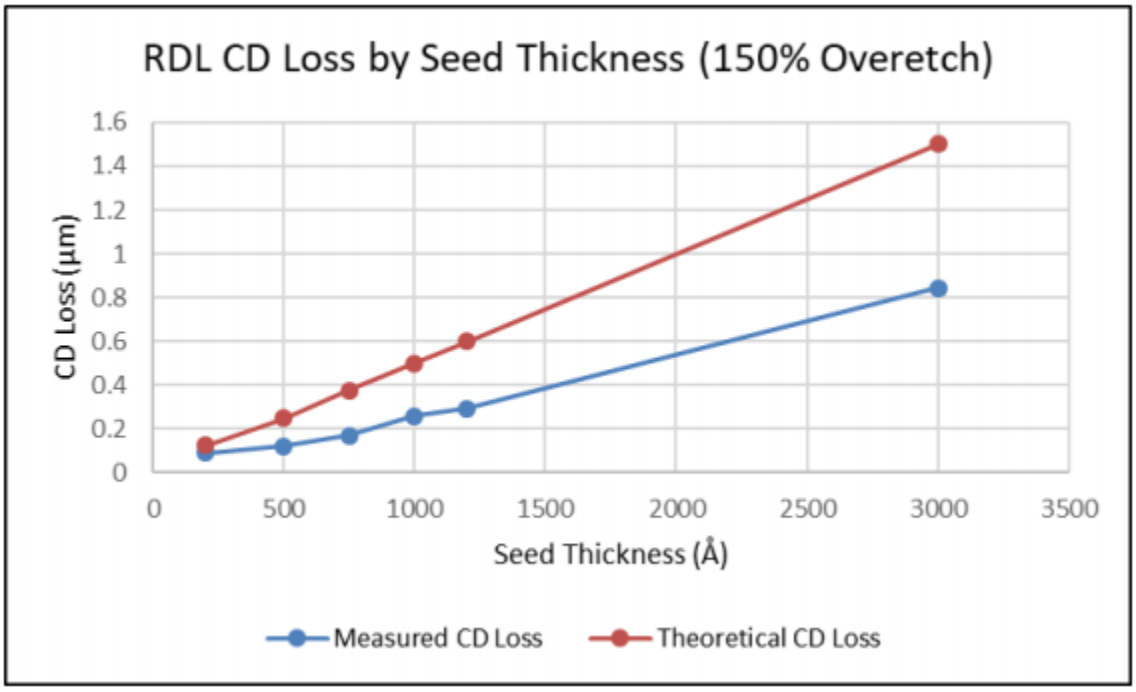


Figure 2-15: Critical dimension (CD) loss of 2 µm line/space RDL with varying seed thicknesses [39]

Planarization of RDL for large panels is another critical step for high yield lithographic patterning of subsequent layers of RDL. Chemical mechanical planarization (CMP) is common for BEOL RDL processes to planarize multi-layer RDL. The introduction of Surface Planar Tool

from Disco for planarization of polymer RDL is a big advantage for scaling multi-layer fine pitch RDL [[41], [42], [43]]. The tool is similar to a mechanical blade where the blade shears off the polymer and copper RDL to obtain a planarized surface. The limitations and considerations to be taken for reliable usage of this tool will be discussed in this study.

Microvia formation is a big challenge in polymer SAP RDL processing. The smallest microvia diameter fabricated is 3-6 µm using a photosensitive polymer dielectric. As shown in Figure 2-12, the taper angles are well below 75^0 during fabrication of small diameter (< 5 µm) microvias [44]. UV laser-based high throughput microvia is currently limited to 20 µm diameter in polymer dielectric [4]. This research proposes novel chemically amplified photosensitive dielectric dry film materials to scale to 2-3 µm diameter microvias. The current processes for microvia formation suggest having the limit of scaling the microvias to 2 µm diameters in 5 µm thick dry film dielectrics with taper angles in the range of 55^0-75^0. However, the research envisaged in this proposal include a new process development to scale the microvia diameters to below 2 µm as well with taper angles closer to 90^0.

2.5 Reliability of multi-layer RDL

The reliability of 2 µm multi-layer RDL is important for polymer SAP RDL. The reliability studies have been focused on two main aspects: (A) Leakage failures between copper traces due to diffusion of copper in polymer dielectrics under biased highly accelerated stress tests (bHAST) (130 ^{0}C, 85% RH and 3.5 Volts), and (B) Thermal cycling reliability of 2 µm diameter microvias. There have been various empirical studies for leakage failures measuring the failure of 1-2 µm line and space structures in different polymer dielectrics after exposing the RDL to bHAST [[44], [45]].

Different metal and inorganic barrier materials have been proposed to prevent these leakage failures [[46], [47]].

The challenge with metal barrier is the requirement to employ a wet etch removal step to remove the high resistance metal barrier from copper capture pads without damaging the copper structures while metallizing the microvias. The challenge with inorganic barrier material like SiN_x is its high dielectric constant leading to increased capacitance between the traces. Thin SiN_x is not shown to be a reliable barrier between copper traces [[46], [47]]. The crack failures due to thin SiN_x layers and the diffusion of copper out of the cracks is shown in Figure 2-16. An alternative thick dual inorganic barrier layer suggests preventing diffusion of copper into the polymer dielectrics as shown in Figure 2-17 [8]. However, as discussed above, the high dielectric constant of this thick inorganic barrier layer nullifies the benefit of low dielectric constant polymer RDL. There is a need for a novel organic barrier with low dielectric constant that can be used to prevent leakage failures. There is an effect of moisture and halogen content in polymer dielectrics on the electrochemical migration of copper lines [47]. A study performed with two different resins, resin (A) with chlorine content of 81.2 ppm and resin (B) with chlorine content of 6 ppm, demonstrate that < 10 ppm halogen content is ideal for 2 µm line width and space RDL [47]. The failure mechanisms are different for both resins, where for resin (A), the copper diffusion is quick and forms dendrites on the copper cathode. For resin (B), the copper diffusion is slow and corroded copper particulates are seen in the polymer dielectrics. The time to failure (TTF) for 2 µm line width and 2 µm space RDL is < 10 hours for resin (A) while > 150 hours for resin (B). This is shown in Figure 2-18. To predict the ideal organic barrier, there is a need to develop a model with the existing polymer dielectrics which have advanced in terms of very low halogen content (< 10 ppm) but still suffer from high moisture content. The Peck, Eyring and Hornung models have been

chosen as references widely to predict corrosion failures in plastic packages [[48], [49], [50], [51]]. The research proposes to develop a model based on these reference models to predict diffusion rate of copper in advanced epoxy-based dielectrics to help identify the ideal material properties of novel organic barrier required to prevent leakage failures for 2 µm RDL traces. The last part of this research is to demonstrate thermal cycling reliability of 2 µm diameter microvias.

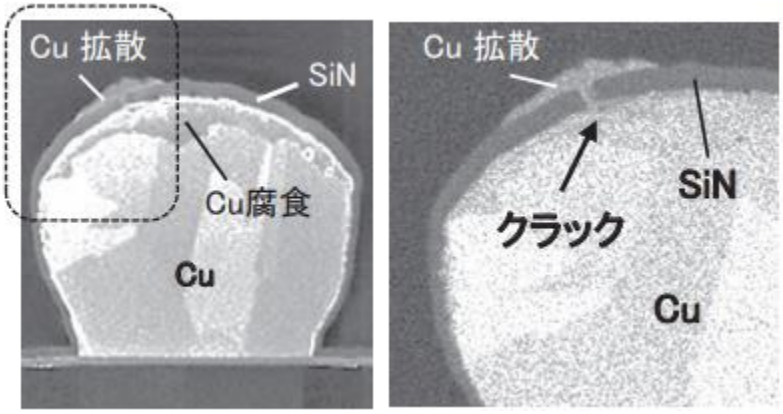


Figure 2-16: Crack in thin (20 nm) SiN_x leading to copper diffusion failures into polymer dielectrics [47]

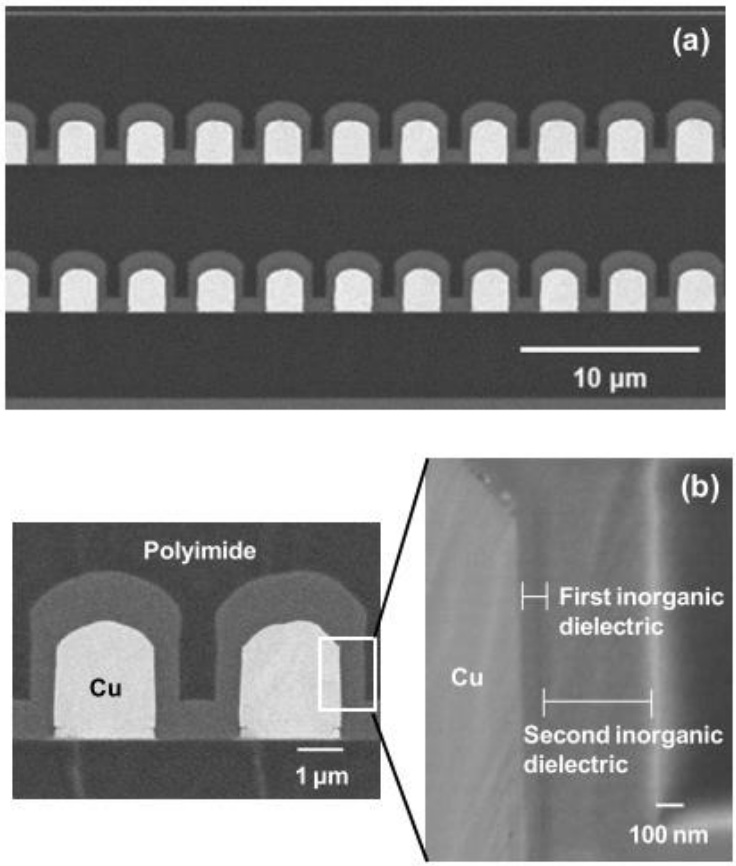


Figure 2-17: Thick dual inorganic barrier layers prevent copper diffusion into polymer dielectrics. Two-thirds of the space between copper lines is covered with high dielectric constant inorganic barrier leading to poor signal integrity and lower bandwidth RDL [8]

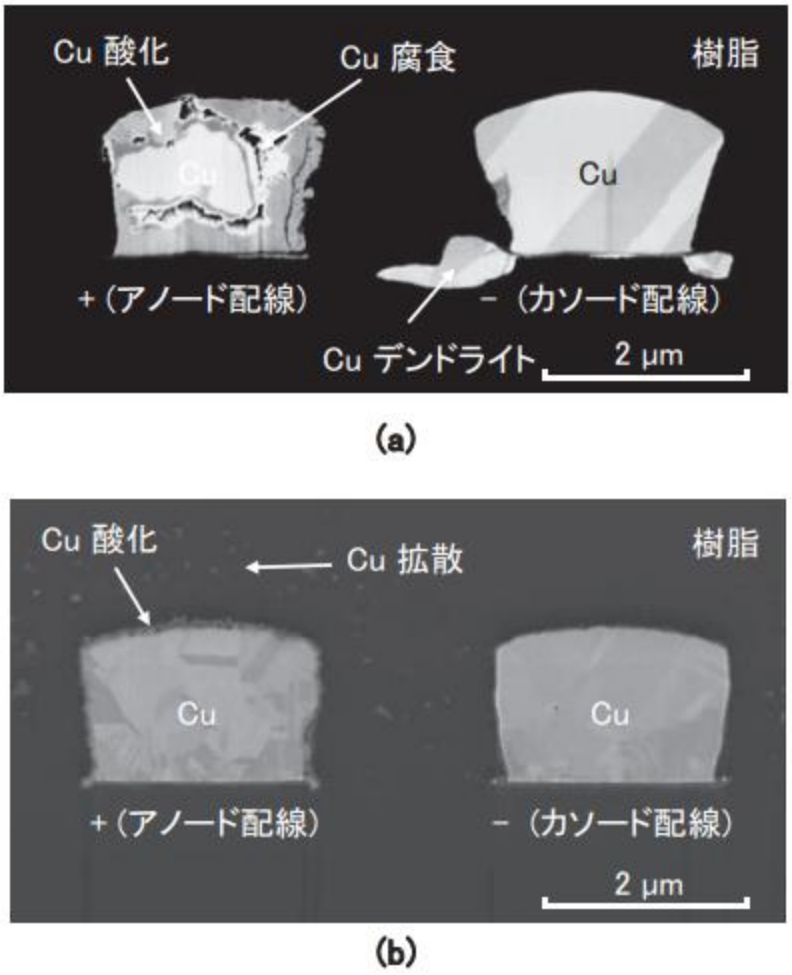


Figure 2-18: Electrochemical migration of copper in 2 μm line width and 2 μm space polymer RDL with (a) Resin A with higher halogen content showing dendritic copper migration failures and (b) Resin B with lower halogen content showing diffusion of corroded copper oxide particles in polymer dielectrics [47]

CHAPTER 3. MODELING FOR LAYER-TO-LAYER REGISTRATION

This chapter describes the characterization of organic laminate and glass core panels for predicting the fundamental limit of capture pad required to land a microvia.

3.1 Technical Approach for Modeling Layer-to-Layer Registration

This research will consider the effect of: (A) Different T_g and CTE organic laminate cores along with low CTE (3 ppm/K) and high CTE (7.8 ppm/K) glass core and, (B) Different percentages of copper RDL on layer-to-layer dimensional shifts. To study the layer-to-layer registration shifts with different core materials, the research proposes to split the problem into two approaches: (i) Characterize the dimensional shift of the bare core material without any RDL copper patterns or any polymer dielectric, (ii) Model and characterize the dimensional shift of core materials with different area densities of copper patterns in the RDL.

To study the first part, a range of advanced organic laminate cores with respect to different T_g, elastic modulus and CTE is chosen along with low CTE glass core.

The laminate materials are manufactured as resin prepregs stacked on to each other along with copper foils and hot pressed and cured to form a laminate. Each prepreg is manufactured by dipping a woven glass fiber cloth in a resin system containing inorganic fillers like silica. This is shown in Figure 3-1. Thus, the laminate material is a composite system of polymer resin, glass fiber weave and silica fillers along with other additives like flame retardants. On the other hand, glass is drawn from the melt of oxides to a homogeneous solid material. A summary of the properties of laminate core materials chosen for this study is summarized in Table 3-1. The variation in T_g is due to the resin system in organic laminate core while the CTE is primarily influenced by the type and % content of glass fibers and amount of silica fillers in the composite

core material. The low CTE BT uses a different grade of low CTE glass fibers like T-glass or S-glass fibers compared to the standard E-glass fibers used in standard BT. Scanning electron microscopy (SEM) is used to characterize and understand the glass weave patterns in different core materials while thermogravimetric analysis (TGA) is used to characterize the amount of % inorganic materials like silica filler and glass fiber in the core material. Cross-sectional SEM will confirm if there are any non-uniformities in X and Y direction of the composite system for the core materials.

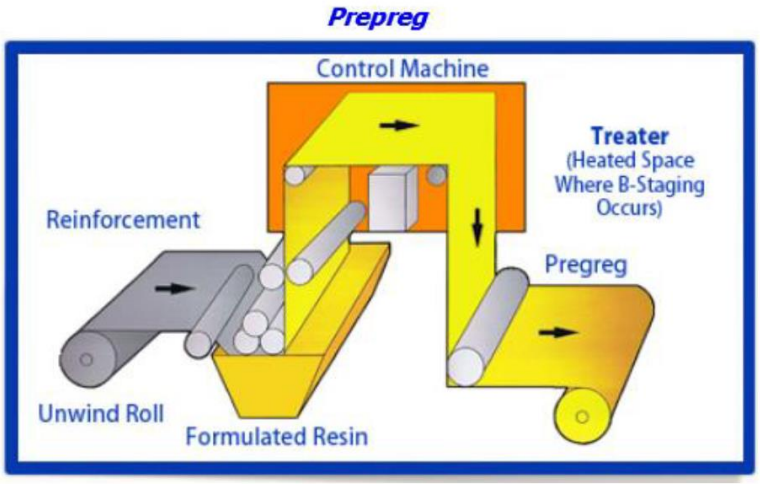


Figure 3-1: Manufacturing of prepregs

Table 3-1: Properties of laminate core materials
(BT stands for Bismaleimide Triazine resin)

Materials	CTE (ppm/K)		T_g	Modulus	Thickness (With Cu foil)	Thickness After Cu removal
	α1	α2				
Standard BT (BT-Epoxy)	14	5	230° C	28 GPa	100 um	75 um
New low CTE, high T_g BT	3	2	270° C	34 GPa	100 um	75 um

3.2 Characterization of dimensional changes in bare core materials (No copper or polymer RDL)

The characterization of dimensional changes is performed by exposing the core materials to solder reflow cycles with a peak temperature of 260 ^{0}C and cooling down under normal atmosphere to room temperature. The high temperature solder reflow cycling is performed under inert nitrogen atmosphere. A co-ordinate measurement machine (CMM) with a traveling microscope is used to characterize the dimensional changes across a 6-inch x 6-inch square panel. The measurement error of CMM is of the order of +/- 5 μm over 100 mm length. The panels are drilled with 300 μm diameter through holes using an IR laser (λ = 1064 nm) on the four corners of each panel. The co-ordinates of the center of the through holes are measured before and after the heat and cool solder reflow cycles. One of the corner holes of the panel is considered as the reference point to measure the relative shifts in dimensions of the panel. The dimensional change study is performed for organic laminate core materials at the following three stages: (A) Removal of copper foil from the copper clad laminate core using a standard copper chloride wet etch process at 45 ^{0}C. (B) Two heat (solder reflow) and cool cycles from 260 ^{0}C to 25 ^{0}C with the bare laminate without any copper foil. (C) Additional two heat and cool cycles from 260 ^{0}C to 25 ^{0}C. BT is the most commonly used resin in advanced organic package substrates today. Table 3-2 summarizes the results of standard BT and novel low CTE, high T_g BT core. The results indicate that the compressive stresses are developed in the sample during the cooling process after hot press curing of BT laminate core with copper foil. These stresses are released during the copper foil etch process causing the samples to expand.

Table 3-2: Expansion in BT substrates after copper foil etch

Laminate Type	Expansion in X-direction (in ppm) (After Cu removal)	Expansion in Y-direction (in ppm) (After Cu removal)
Standard BT	Mean: + 250.3 Std. Dev: 6.2	Mean: +116.3 Std. Dev: 14.7
High T_g, low CTE BT	Mean: + 561.6 Std. Dev: 52.5	Mean: + 552.5 Std. Dev: 50.1

Table 3-3 summarizes the shrinkage in BT substrates after exposure to solder reflow cycles. The shrinkage behavior clearly indicates that there is incomplete curing in BT laminate core which was also confirmed in reference [15] for PCB laminate core using differential scanning calorimetry (DSC) studies. The average shrinkage for standard BT laminate core is ~ 315 ppm in X-direction while ~ 170 ppm in Y-direction. For high T_g, low CTE advanced BT laminate core, the average shrinkage is ~ 400 ppm in X-direction while ~ 200 ppm in Y-direction. The possible explanation for higher shrinkage in high T_g, low CTE advanced BT laminate core may be due to similar manufacturing temperatures (~ 180-200 ^{0}C) used for both BT laminate cores. The manufacturing process requires hot press with copper foils to manufacture laminate cores and the higher pressures decrease the free volume between chains of BT-epoxy resin, reducing their mobility and freezing the curing reaction at lower conversions [16]. For a higher T_g laminate core, the curing reaction will be more incomplete than a lower T_g laminate core. As the copper foil is etched away, the compressive stresses are fully released, and this helps in post-curing process. This is confirmed in Table 3-3, where the shrinkage after two additional solder reflow cycles is minimal compared to

the shrinkage observed after first two solder reflow cycles. After two additional solder reflow cycles, the average shrinkage for standard BT was only ~ 17 ppm in X-direction and ~ 45 ppm in Y-direction while for high T_g, low CTE advanced BT laminate core, it was ~ 26 ppm in X-direction and ~ 66 ppm in Y-direction. The shrinkage study was also studied for a low CTE glass core and there was no measurable dimensional change in glass core on exposure to solder reflow cycles. This was expected as glass is a homogeneous solid material with $T_g > 500\ ^0C$ and the solder reflow cycle with a peak temperature of 260 ^0C is far below the T_g of glass core.

Table 3-3: Shrinkage in BT substrates (- ve sign denotes shrinkage) on exposure to solder reflow cycles

Laminate Type	Shrinkage in X-direction (ppm) (After 2 solder reflow cycles) (- ve sign denotes shrinkage)	Shrinkage in Y-direction (ppm) (After 2 solder reflow cycles)	Shrinkage in X-direction (ppm) (After 4 solder reflow cycles)	Shrinkage in Y-direction (ppm) (After 4 solder reflow cycles)	Shrinkage in X-direction (ppm) (After 4 solder reflow cycles) (calculated w.r.t dimensions after 2 solder reflow cycles)	Shrinkage in Y-direction (ppm) (After 4 solder reflow cycles) (calculated w.r.t dimensions after 2 solder reflow cycles)
Standard BT (Without Cu foil)	Mean: - 316.7 Std. Dev: 2.5	Mean: - 171.7 Std. Dev: 12.3	Mean: - 302.2 Std. Dev: 40.1	Mean: - 226.2 Std. Dev: 5.1	Mean: - 17.2 Std. Dev: 8.5	Mean: - 44.8 Std. Dev: 4.3
High T_g, low CTE BT (Without Cu foil)	Mean: - 407.7 Std. Dev: 3.9	Mean: - 196.2 Std. Dev: 5.7	Mean: - 454.5 Std. Dev: 23.5	Mean: - 268.7 Std. Dev: 7.3	Mean: - 25.8 Std. Dev: 5.3	Mean: - 65.9 Std. Dev: 13.9

The above study suggests that multiple solder reflow cycles of laminate core after etching away the copper foil can induce almost near-complete curing process. This process can make the laminate core less prone to severe dimensional changes due to any post-curing during thermal excursions. To confirm this, thermo-mechanical analysis (TMA) was also performed to

characterize dimensional changes for heat and cool cycles from 25 ^{0}C to 260 ^{0}C with the core materials.

TMA studies were done on the core materials to confirm the shrinkage patterns. For laminate core materials, both copper cladded and copper foil etched away core substrates were used for TMA studies. The samples were heated from 25 ^{0}C to 260 ^{0}C at a rate of 20 ^{0}C/min and cooled under N_2 atmosphere at a rate of 5 ^{0}C/min for all the materials. As shown in Figure 3-2, the glass core showed a dimensional change of < 2.5 µm. Figure 3-3 and Figure 3-4 show the dimensional changes in copper-cladded new low CTE BT and standard BT laminate core materials. For standard BT, two heat and cool cycles were performed to confirm the lowering in shrinkage with post-curing process during the second heat and cool cycle. Also, a TMA run was conducted with the standard BT core exposed to three cycles of solder reflow oven at a peak temperature of 260 ^{0}C. The result is shown in Figure 3-5 for standard BT which have been exposed to five heat and cool cycles during this entire process. By the fifth heat and cool cycle, the copper-cladded standard BT shows dimensional change similar to that of glass. The result was similar as shown in Figure 3-7 for copper foil-etched standard BT where the TMA result showed similar dimensional change to the first TMA run in Figure 3-5. This trend was similar for low CTE, high T_g BT as shown in Figure 3-7. To confirm that there is no shrinkage due to any moisture absorption, thermogravimetric analysis (TGA) studies (25 ^{0}C to 260 ^{0}C) were performed on all the core materials which showed < 0.1 wt.% loss suggesting no shrinkage due to water absorption.

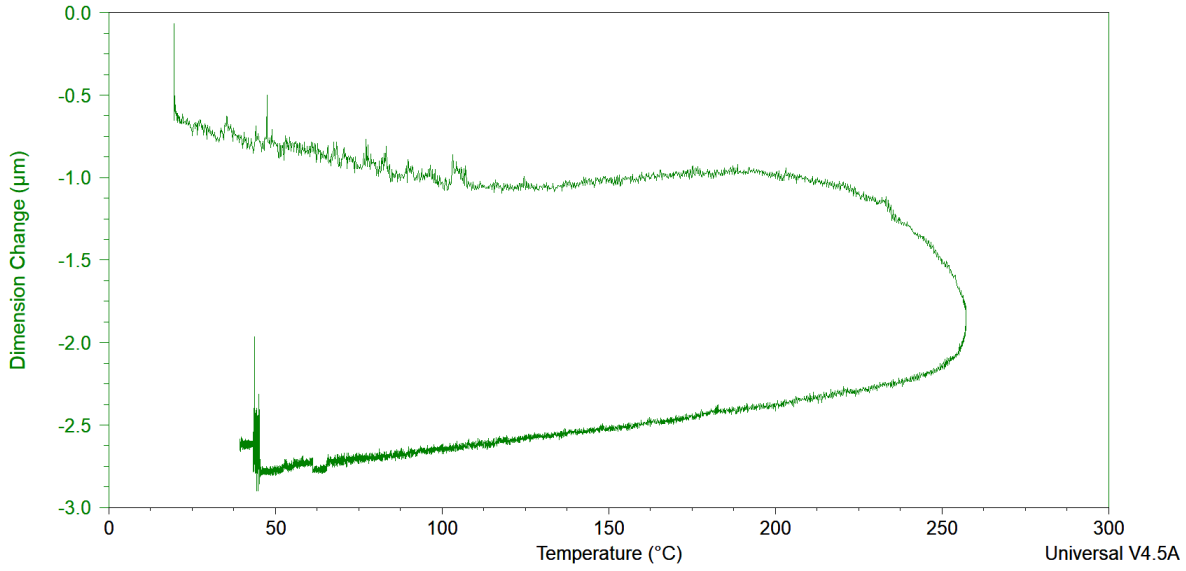


Figure 3-2: Dimensional change after first heat and cool cycle- Low CTE glass

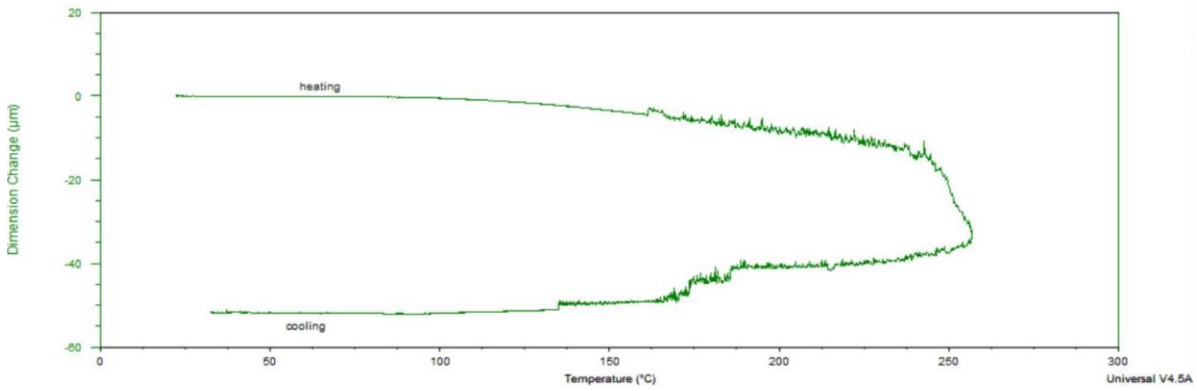


Figure 3-3: Dimensional change after first heat and cool cycle- Copper-cladded new low CTE BT

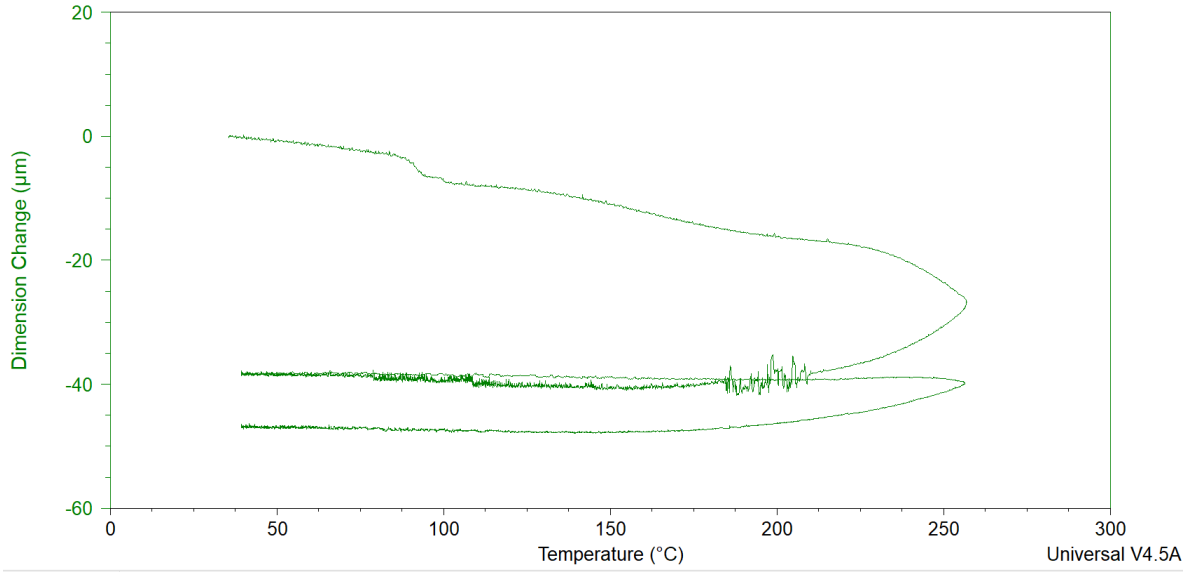


Figure 3-4: Dimensional change with two heat and cool cycles in TMA- Copper-cladded standard BT

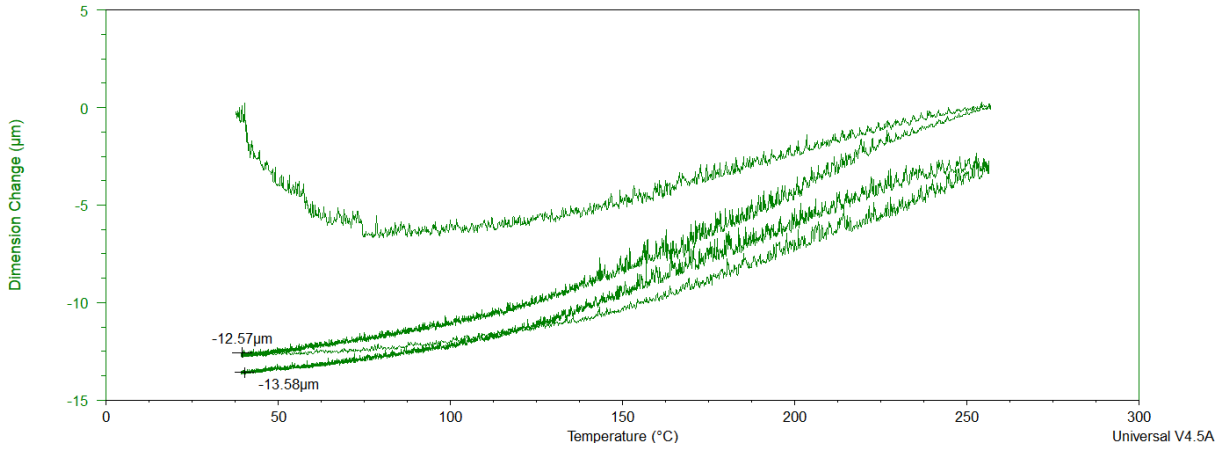


Figure 3-5: Dimensional change with two additional heat and cool cycles in TMA for copper-cladded standard BT pre-exposed to a heat treatment of three solder reflow cycles at a peak temperature of 260 ^{0}C

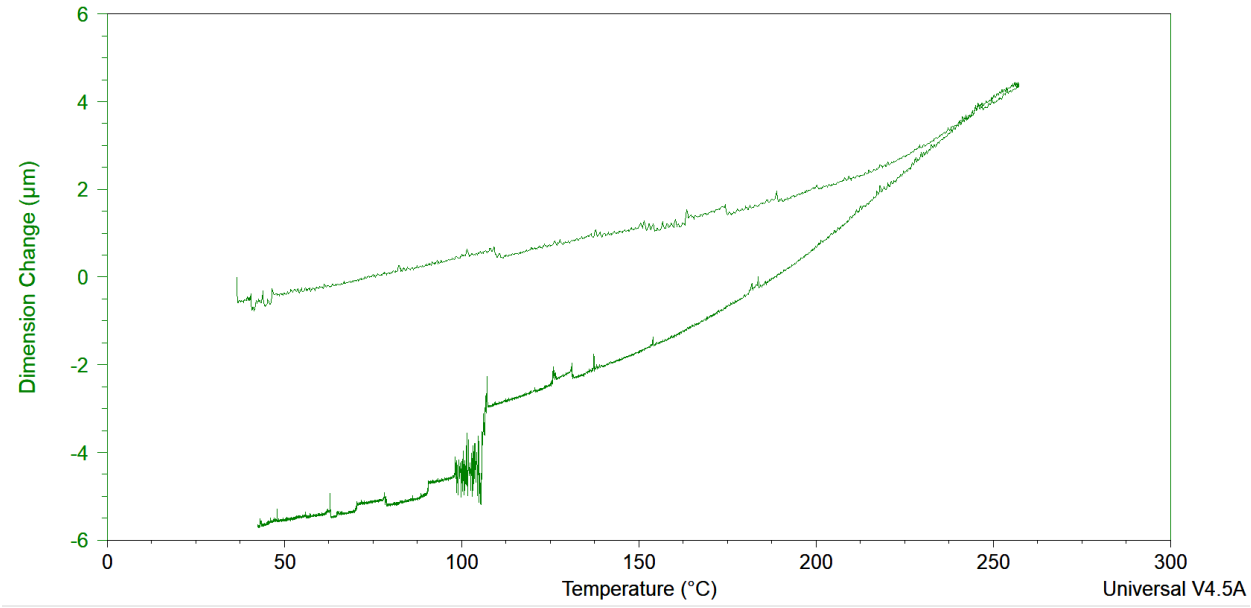


Figure 3-6: Dimensional change with an additional heat and cool cycle in TMA for copper foil-etched standard BT pre-exposed to a heat treatment of three solder reflow cycles at a peak temperature of 260 ^{0}C

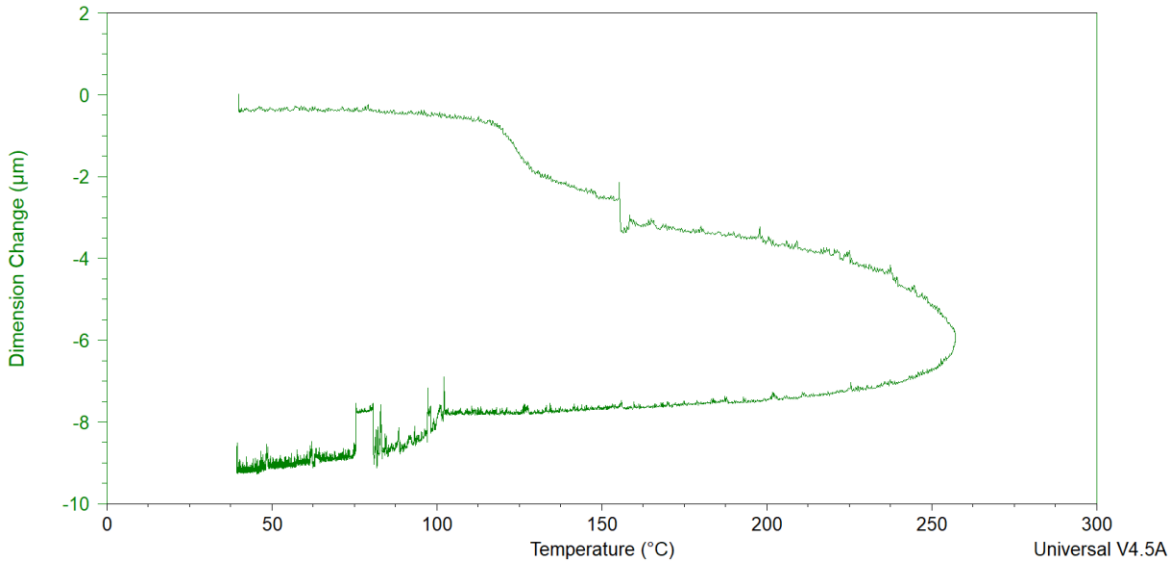
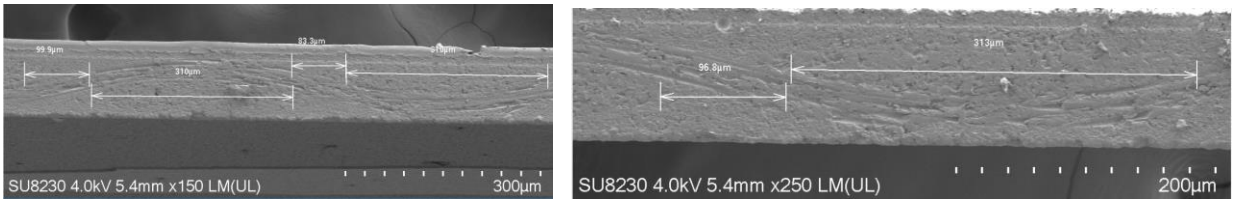


Figure 3-7: Dimensional change with an additional heat and cool cycle in TMA for copper foil-etched new low CTE, high T_g BT pre-exposed to a heat treatment of three solder reflow cycles at a peak temperature of 260 ^{0}C

3.3 Cross-sectional Scanning Electron Microscopy (SEM) characterization of laminate core materials

Cross-section SEM imaging was done to understand the non-uniform behavior shrinkage patterns in X and Y directions of the BT laminate core materials. Figure 3-8 shows minor variations in the structures of low CTE, high T_g BT laminate in X and Y directions. Figure 3-9 shows the thickness of a glass fiber bundle is ~ 45 µm. In high T_g BT, as mentioned before, a low CTE grade glass fiber like T-glass or S-glass is used compared to the standard E-glass fiber in standard BT. For standard BT, the only difference is that the glass fiber bundle is thinner (20-30 µm) and hence, two glass fiber weaves are seen in cross-sectional images in Figure 3-10 and Figure 3-11. This suggests that there are two thin prepreg layers used to make the final laminate in standard BT. For both BT laminate core, the total thickness of glass fibers observed across a 100 µm thick core is ~ 80 µm. Thus, the structures are not drastically different in X and Y directions for both BT laminate cores apart from minor differences in thickness (within +/- 10%) or in the width or pitch between glass fiber bundles (within +/- 10%).



(X-direction) (Y-direction)

Figure 3-8: New low CTE, high T_g BT in X and Y directions (with one glass fiber bundle cross-woven across the thickness and the width of one glass fiber bundle is ~ 300 µm)

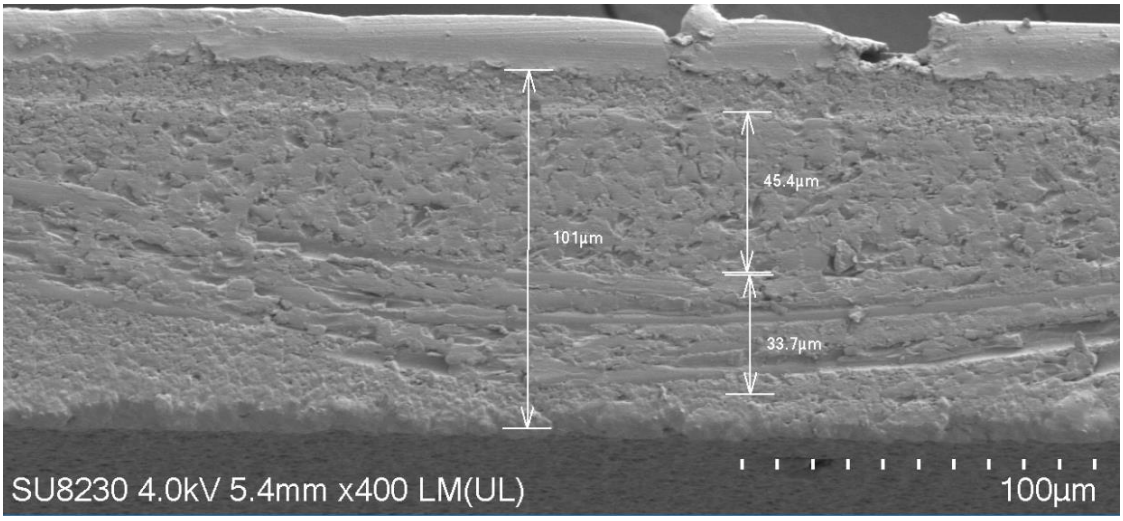


Figure 3-9: New low CTE, high T_g BT in X-direction (Zoomed Image shows the total height of glass fibers to be ~ 80 µm for 100 µm thick core).

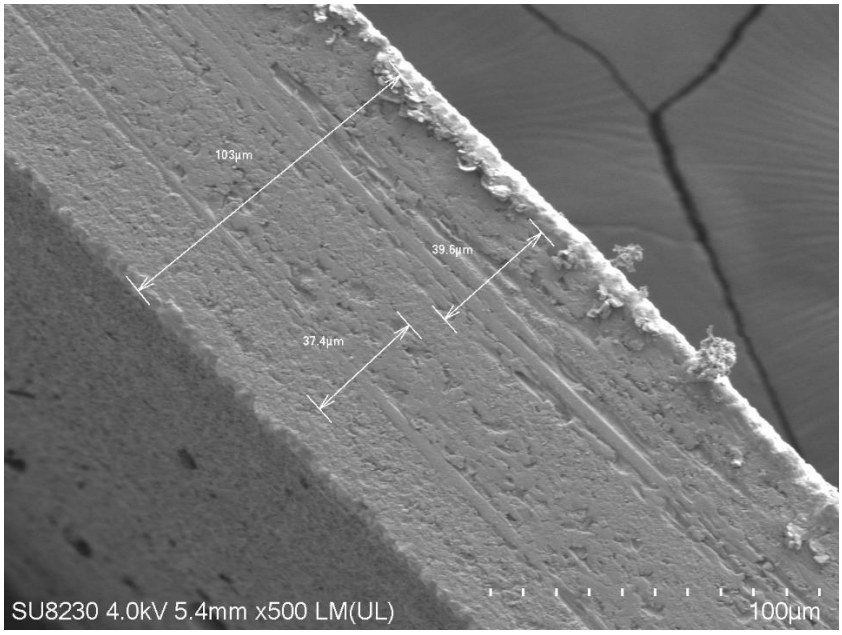


Figure 3-10: Standard BT in X-direction revealing two glass fiber weaves cross-woven across the thickness and the total height of glass fibers is still 80 µm for 100 µm thick core. This suggests there are two thin prepregs used to make the final laminate.

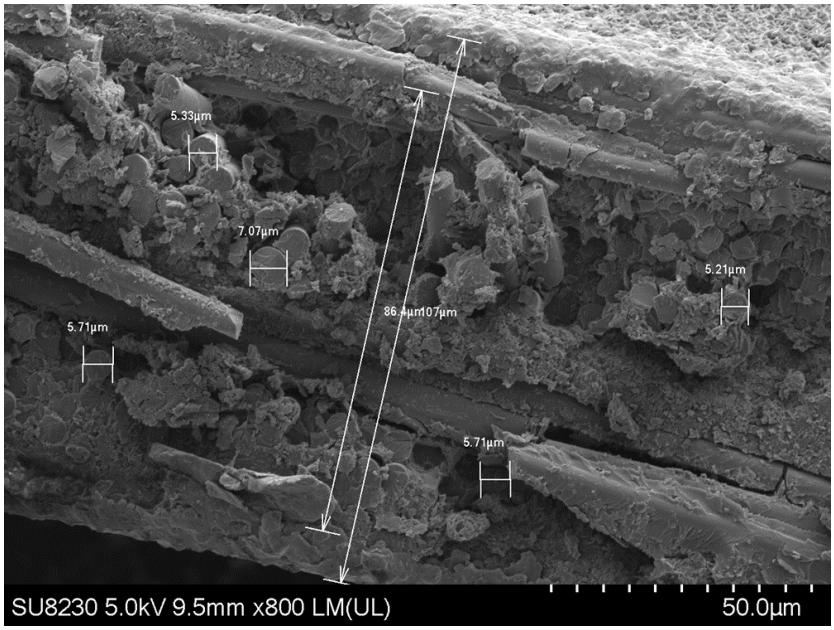


Figure 3-11: Standard BT in Y-direction revealing similar structure of two glass fiber weaves cross-woven across the thickness and the total height is ~ 80 µm.

The weaving pattern of glass fibers in both BT laminate cores seem to be a regular $0^0/90^0$ warp and weft pattern in a plain weave form as shown in Figure 3-12. The stretching ability of warp and weft patterns are different in the final laminate and this might be the cause for different shrinkage behavior in X and Y directions for the laminate core. Dynamic mechanical analysis (DMA) studies performed in standard BT core reveal no change in modulus of the BT core in X and Y directions as shown in Figure 3-13. This confirms the hypothesis that there are no major chemical or compositional changes for the BT laminate core in X and Y directions.

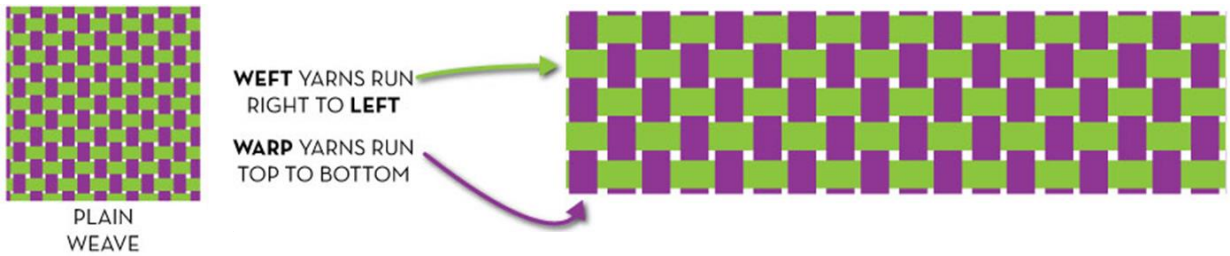


Figure 3-12: Warp and Weft glass weaving pattern in laminate core

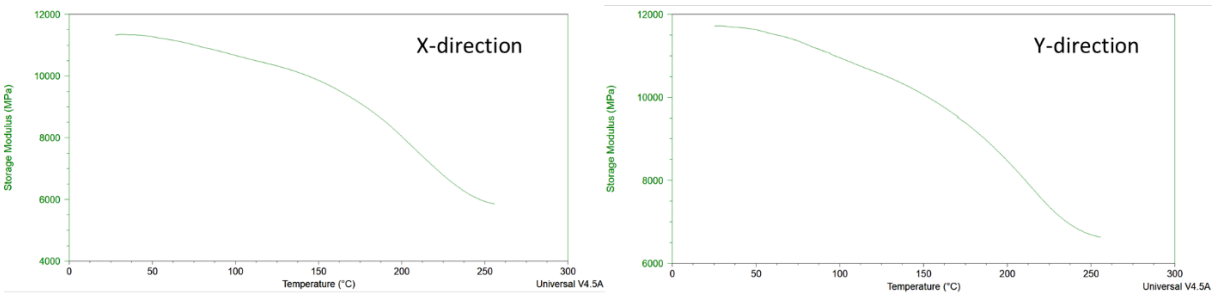


Figure 3-13: DMA plots of standard BT reveal similar elastic modulus behavior versus temperature in both X and Y directions

3.4 Modeling and characterization of dimensional changes with varying copper area densities in RDL patterns

For part (ii) of the study, finite element modeling (FEM), using ANSYS Mechanical APDL, was used to model different area densities of copper patterns on to the core substrate. The model was created for two and four layers of copper RDL as shown in Figure 3-14. A finite element analysis (FEA) model with birth and death approach was used to characterize dimensional change in substrates during sequential processing of RDL. To simplify the model, copper was considered as a rectangular block and simulated for different % area densities. Also, a model with copper circular pads was simulated to compare with the rectangular block model for low CTE glass core. For this, the design structure of copper pads was imported from AUTOCAD to SOLIDWORKS and the core, dielectric and copper pads were assembled in SOLIDWORKS to form the RDL stack. This model was simulated using ANSYS Workbench with the same APDL codes to obtain the dimensional shifts. The results were found to be similar (within 5 %) to the model with copper as a rectangular block. Taking into consideration the computation time, the results were generated with the simplified model considering copper as a rectangular block in this study. Glass and copper were modeled as elastic materials and dynamic mechanical analysis (DMA) was used to characterize elastic modulus versus temperature properties of organic laminate core and polymer dielectrics.

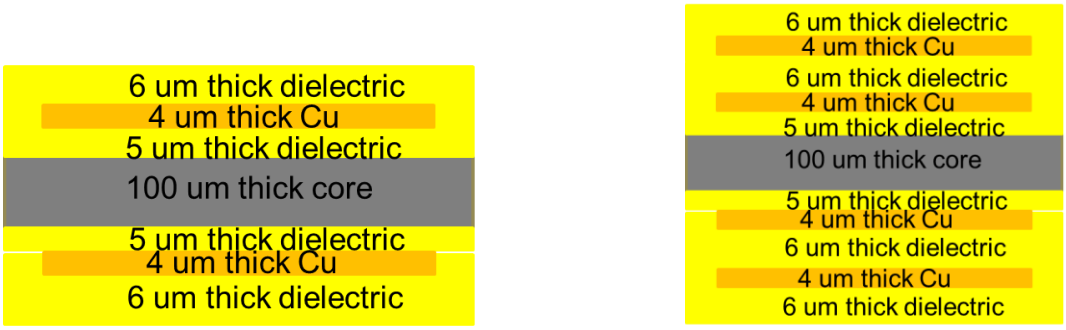


Figure 3-14: RDL stack-ups for modeling of layer-to-layer registration

The standard T_g BT, new low CTE BT, FR-4, low CTE (3.8 ppm/K) and high CTE (7.8 ppm/K) glass core materials were first characterized using DMA for elastic modulus as a function of temperature. For the laminate core materials, the copper foil was first etched away from the laminate core using copper chloride etch solution and baked in a N_2 oven at 125 ^{0}C for 12 hours to remove any moisture. The DMA studies were performed as per the specifications for sample thicknesses in the range of 0.02-1 mm, keeping the width at around 5 mm, free length at 10 mm and heating from 25 ^{0}C to 260 ^{0}C at a rate of 5 ^{0}C/min [52]. The measurement results are shown in Figure 3-15 and Figure 3-16.

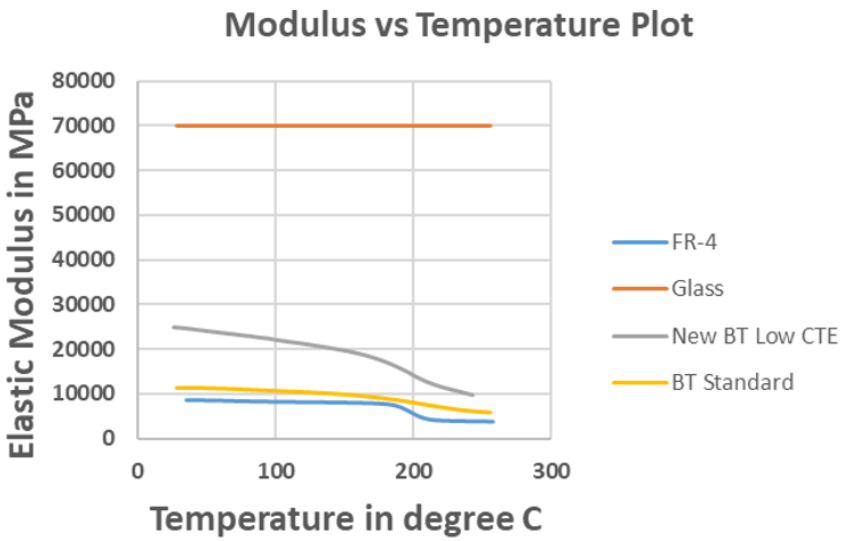


Figure 3-15: Modulus vs Temperature plots for different core materials using DMA

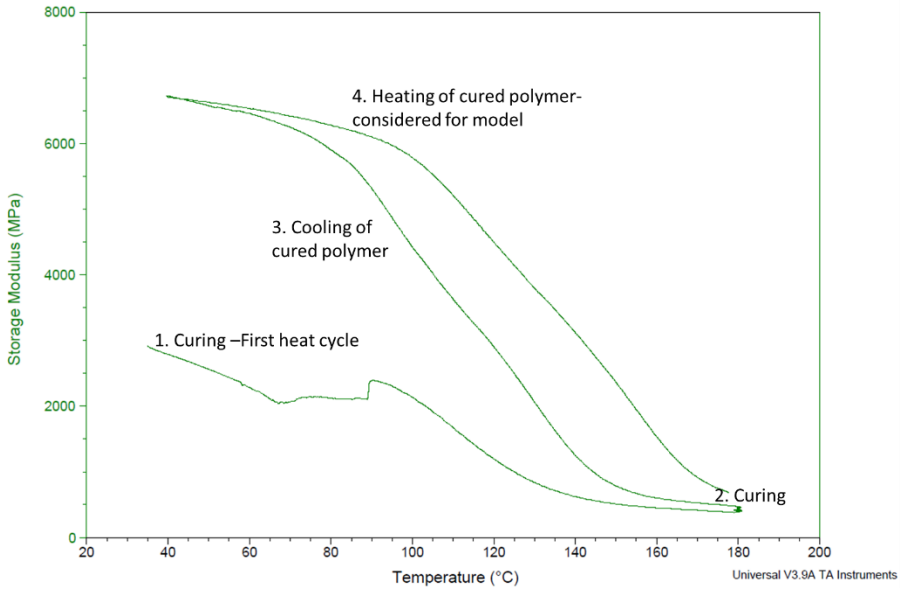


Figure 3-16: DMA profile of cured polymer dielectric (Step 4 properties are used for the model)

The next step is to characterize the effect of changing % area density of RDL copper patterns on to the glass substrate. This study was primarily done by finite element modeling since it is difficult to precisely fabricate high area density copper patterns without variations in

thicknesses leading to warped panels. The warped panels lead to non-reproducible shrinkage patterns during the heat and cool cycles. For finite element modeling, two metal and four metal layers of RDL on different core panels were studied. The geometry of the stack-up is a simplified one as shown in Figure 3-14. The material properties are shown in Table 3-4 and the dimensional changes are considered while cooling the sample from 150 ^{0}C to 25 ^{0}C. The stress-free temperature is chosen to be 150 ^{0}C because the T_g of the polymer dielectric in the stack-up is around 150 ^{0}C and there is negligible stress in the substrate above 150 ^{0}C. Quarter symmetry is applied for the entire geometry and a birth and death model is used to simulate sequential processing. Considering an example of two-layer RDL geometry, the entire geometry is first killed (death) excluding the core material and heated to 150 ^{0}C in step 1. In steps 2 and 3, the 5 μm thick polymer dielectric is introduced (birth) and the entire structure is cooled to 25 ^{0}C, mimicking the cooling process with cured polymer. The stresses due to curing shrinkage of advanced ultra-thin, low modulus polymer dielectric are not considered in the model. In step 4, the entire structure is again heated to 150 ^{0}C and 4 μm thick copper layer is introduced (birth) and cooled down to 25 ^{0}C in step 5, mimicking the annealing process after copper electroplating. The next step 6 involves heating the structure to 150 ^{0}C, followed by the birth of next layer of polymer dielectric (4 μm thick around the copper plus 6 μm thick on top of the copper layer) and cool down to 25 ^{0}C in step 7, mimicking the cooling process with cured polymer. The cool down of the entire RDL with the second layer of polymer dielectric leads to dimensional changes in the location of copper pad. This mimics the net dimensional change (difference in dimensions between steps 5 and 7) of copper pads.

Table 3-4: Material properties for FEM model

Material	Thickness (in µm)	Coefficient of Thermal Expansion (CTE) (in ppm/K from 25-150 ^{0}C)	Elastic Modulus (GPa)	Poisson's Ratio
Low CTE glass	100	3.4	70	0.22
High CTE glass	100	7.8	70	0.22
FR-4	100	20	As derived from the plot of Figures 17 and 23	0.2
Standard BT organic	100	10		0.2
New Low CTE BT organic	100	3		0.2
Polymer dielectric	5, 10 (4 +6)	39		0.34
Copper	4	17		0.33

The results of maximum displacement of copper pads in terms of ppm (shrinkage in µm for 1 m panel length) for each core material with two layers of RDL are plotted in Figure 3-17. The results are plotted for both two layers and four layers of copper RDL. The effect of change in core thickness from 100 µm to 300 µm is also studied. These are plotted in Figure 3-18 and Figure 3-19. The typical area densities in copper RDL for high density 2.5D interposers range from 70-75% in fine pitch copper RDL layers to 80-85% in power plane copper RDL layers close to the laminate core. With these values, the dimensional changes are around 115 ppm, 120 ppm, 140 ppm and 160 ppm for high CTE glass, low CTE glass, low CTE BT and standard BT laminate core materials respectively at 80 % copper area density for four layers of RDL using 100 µm thick core materials. The numbers are a little higher for 300 µm thick core for four layers of RDL because of the fact that for thinner core, the average CTE of the substrate (core + copper RDL layers) is higher than that of the thicker core, leading to lower CTE mismatch with the top layers of RDL.

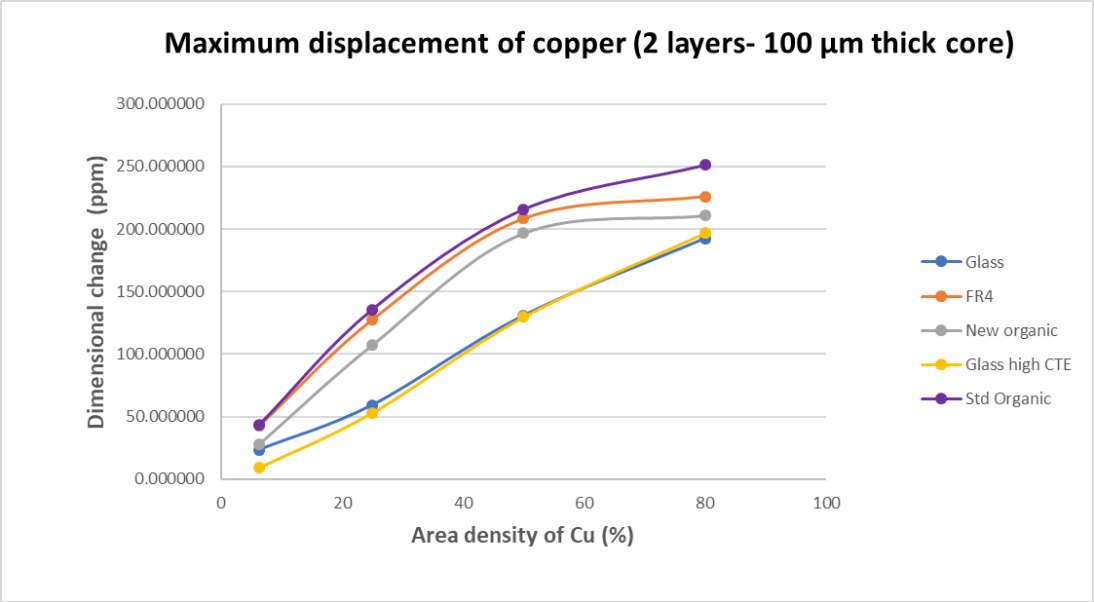


Figure 3-17: Dimensional change (in ppm) for two layers of RDL with different core materials of 100 µm thickness [Glass refers to low CTE glass]

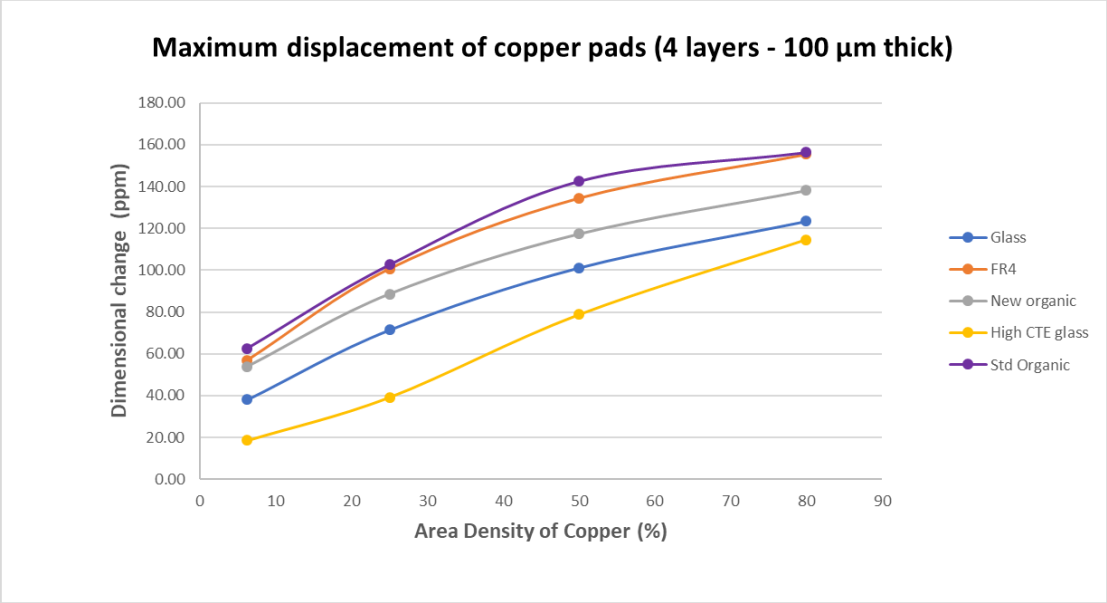


Figure 3-18: Dimensional change (in ppm) for four layers of RDL with different core materials of 100 µm thickness [Glass refers to low CTE glass]

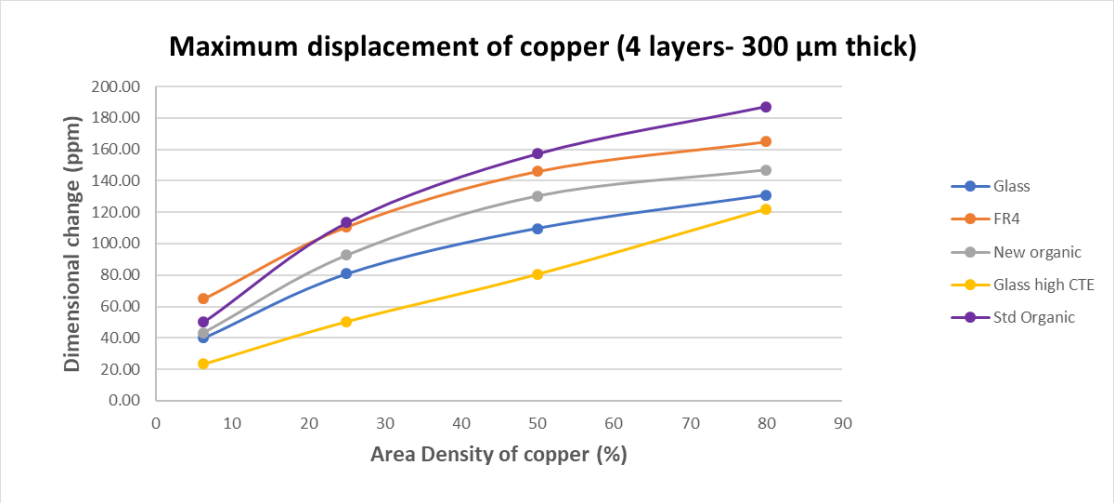


Figure 3-19: Dimensional change (in ppm) for four layers of RDL with different core materials of 300 µm thickness [Glass refers to low CTE glass]

To validate these models, samples with two layers of RDL layer were fabricated with an actual RDL design (equivalent to 25% copper area density). As mentioned previously, higher area density patterns can lead to warpage and the dimensional change results are not reproducible. Hence, a lower 25 % copper area density RDL design pattern was chosen. The dimensional shifts in ppm were measured by the automatic optical inspection of the excimer laser tool during microvia drilling process. Four glass panels (S1, S2, S6, S7) and one organic laminate panel using standard BT organic core were used for this study. All the core materials were 100 µm thick. The copper foil of the standard BT organic laminate core was etched away, and the core material was exposed to three solder reflow cycles before the fabrication process. The results during process, as shown in Figure 3-20, reveal that the copper thickness of first layer RDL was around 3-4 µm (polymer thickness of 6-7 µm). The stack-up was designed for a copper area density of 25% and the thicknesses matched similar to Figure 3-14 for two-layer RDL. The polymer curing temperature was 180 ^{0}C for 1 hour and the copper annealing temperature was 190 ^{0}C for 90 mins. The results of the measured dimensional shifts (in ppm) for glass and organic laminate panels are

shown in Figure 3-21. The microvia diameter in this case is 8 µm and the capture pad diameter is 18 µm and the microvias are drilled without any compensation or auto-scale function in the excimer laser tool. The experimental results from the model match for glass (50 ppm for two-layer RDL with 100 µm thick core at 25 % copper area density) while there is deviation of 15 ppm for standard BT organic from the model (expected is 135 ppm for two-layer RDL with 100 µm thick core at 25 % copper area density). This deviation can be from the organic core movement itself due to curing shrinkage that was predicted in Table 3-3. The non-uniform dimensional shifts seen in organic laminate core can be due to the previously explained different warp and weft behaviors of glass fibers or due to the variation in copper area densities across the panel. As seen in Figure 3-17, the dimensional change in low modulus BT laminate core fluctuates from ~ 100 ppm to ~ 150 ppm for a change in area density from 20 % to 30 %. Based on these results, for an excimer laser scan area of 50 mm x 50 mm, 50 ppm dimensional change in glass core results in 2.5 µm overlay accuracy for glass while 150 ppm dimensional change in standard BT laminate core results in 7.5 µm overlay accuracy for the BT laminate core. These results are shown in Figure 3-21.

Panel ID	Side	Fluence	# of pulse	Polymer thickness	
				8um via	60um via
S-1	1	REE	24	~4	~6
	2	REE	24	5~6	~7
S-2	1	REE	24	6~7	~8
	2	REE	24	~8	~8
S-6	1	REE	22	~7	~7
	2	REE	22	6~7	~8
S-7	1	REE	24	6~7	~8
	2	REE	24	6~7	~8
Organic Dummy	1	REE	24	6~7	6~7
	2	REE	24	6~7	6~7

Figure 3-20: Thickness measurements before laser drilling confirm 3-4 µm thick plated copper and 6-7 µm thick dielectric above the plated copper

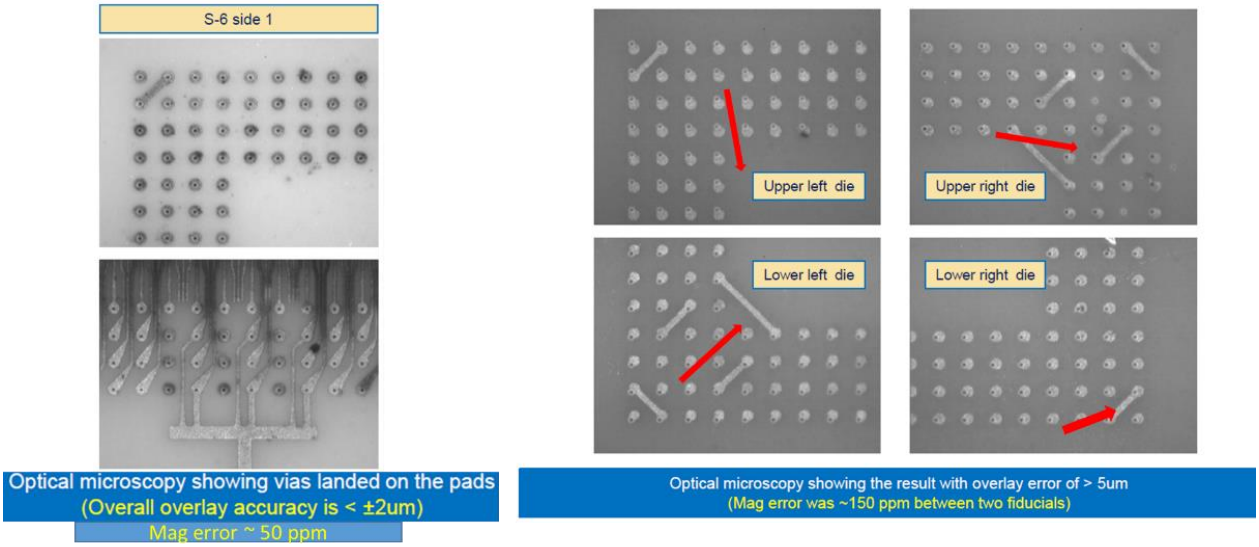


Figure 3-21: The overlay accuracy without any compensation for excimer laser scan area of 50 mm x 50 mm (50 ppm in glass and 150 ppm in standard BT). The dimensional shifts in standard BT across the four corners are non-uniform as confirmed in Table 3-3 with varying shrinkage behavior in X and Y directions. [Courtesy: Yuya Suzuki, Taiyo Ink and Habib Hichri, Suss Microtec]

A second experiment to build four-layer RDL structure was performed without any solder reflow cycle treatment in standard BT laminate core. The expected deviation in this case was 300 ppm due to the curing shrinkage (Table 3-3) and 135 ppm due to copper RDL (Figure 3-17), resulting in a total of 435 ppm dimensional change. A projection stepper with an exposure area of 70 mm x 70 mm was used which can auto-scale and compensate for 0.075 % (25 µm) shrinkage. For an area of 70 mm x 70 mm, 435 ppm dimensional change is equivalent to 30 µm and thus, a 5 µm shift can be observed. This is shown in Figure 3-22. For glass core, the only expected dimensional change is of 100 ppm (equivalent to 7 µm for 70 mm x 70 mm area) and hence, with auto-compensation, there is no dimensional change in the glass substrate as shown in Figure 3-23.

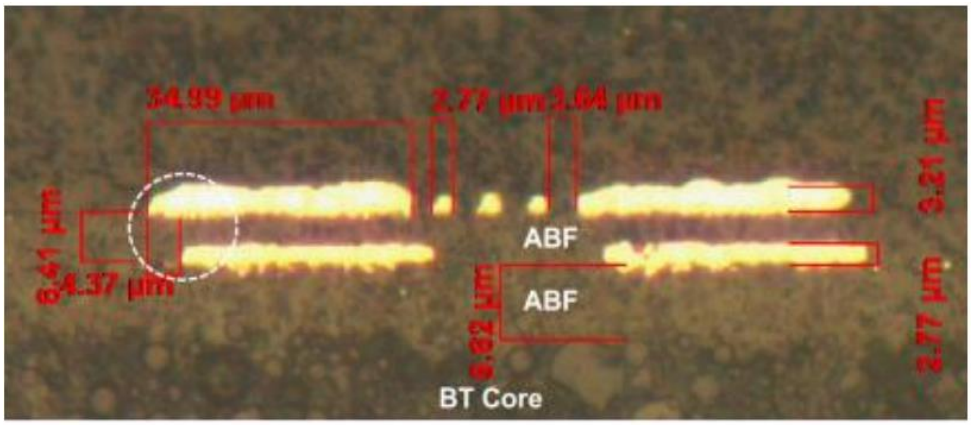


Figure 3-22: Dimensional change of 4.4 µm observed with four-layer RDL structure using standard BT core after auto-compensation in the projection stepper tool

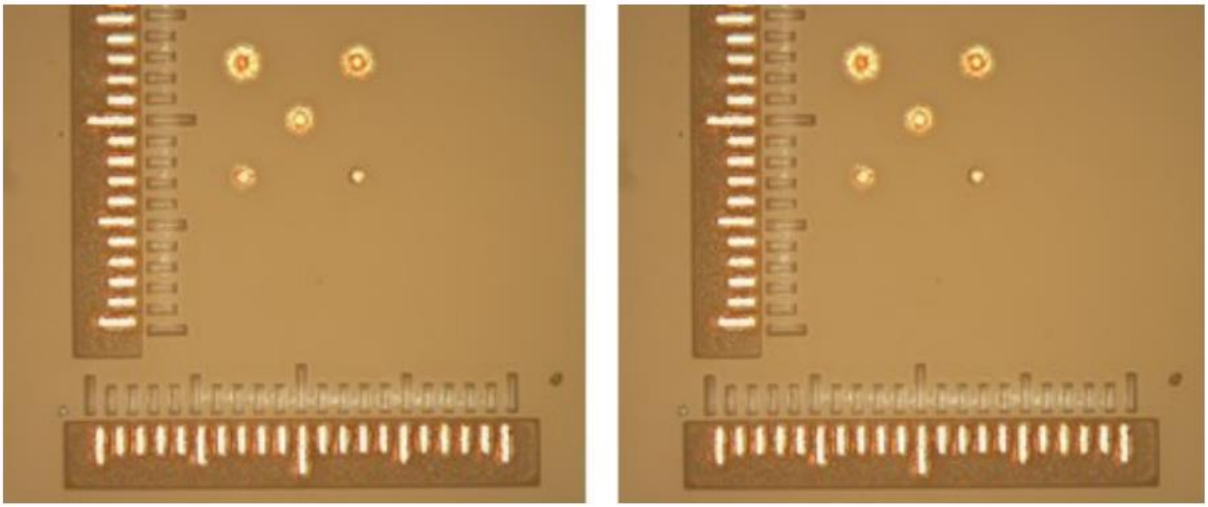


Figure 3-23: Two well aligned Vernier marks (offset is around 0.4 µm) after auto-compensation with the same projection stepper tool in four-layer RDL structure using low CTE glass core

3.5 Chapter 3 Summary

The chapter gives a deep understanding of the parameters affecting the dimensional change in core materials. Table 3-5 below summarizes the minimum capture pad required for laminate versus glass core materials based on the results in this chapter.

Table 3-5: Minimum Capture Pad required for different laminate core materials

Core	Dimensional change from model for 80% copper area density (ppm)	Core shrinkage (ppm)	Total dimensional change (ppm)	For 100 mm x 100 mm exposure shot (Litho Tool can compensate 35 um shrinkage)	For 20 mm x 20 mm exposure shot (Litho Tool can compensate 7 um shrinkage)
Std BT organic	160	300	460	+/- 11 µm	+/- 2.2 µm
New BT organic	140	400	540	+/- 19 µm	+/- 3.8 µm
Low/ High CTE glass	120/ 110	-	120/ 110	Not needed	Not needed

CHAPTER 4. DESIGN FOR 2 MICRON MULTI-LAYER POLYMER RDL

This chapter describes the optimized design of fine pitch polymer RDL required for highest signal integrity and bandwidth performance for 2.5D glass interposer system. The eye diagram will be used to characterize the signal efficiency at different signal data rates for a polymer RDL with parylene-F dielectric ($D_k \sim 2.4$ and $D_f \sim 0.003$) comparing to a silicon BEOL RDL with silicon dioxide dielectric ($D_k \sim 3.9$ and $D_f \sim 0.002$). As noted in section 2.2, the I/O wiring density is critical for 2.5D interposer system and the goal is to design a system with high bandwidth, low delay RDL at the same line pitch of 4 µm to maintain the same I/O wiring density of > 200 IOs/mm/layer for 2.5D glass interposer.

4.1 Geometry for design simulation comparing glass polymer RDL versus silicon SiO_2 RDL

The structure for simulating the graphical processing unit (GPU) to high bandwidth memory (HBM) is shown in Figure 4-1. The open area consists of channels (or copper lines) in stripline configuration. In the open area, the center channel line is marked as a victim surrounded by four aggressors. During simulation, all the five channels will be given random signals (0 to 1 V or 0 to -1 V) for many iterations. The victim and aggressors in the bump area are also shown in Figure 4-1. The eye diagram will be generated based on these signals for a given frequency (or signal data rate) using Advanced Design System (ADS) software. The worst signal performance from the random signaling will represent the inner of the eye and the best signal performance will represent the outer of the eye. The RLGC (resistance, inductance, conductance and capacitance) and S-parameters will be extracted using ANSYS HFSS (High frequency structure simulator) and the biggest contributing factor to the signal losses will be predicted. The geometric parameters for the entire structure are enlisted in Table 4-1. For the polymer RDL, the dielectric thickness is assumed

to be 1 µm to compare the performance with silicon SiO_2 RDL. The aspect ratio of 2 µm width copper line is assumed to be 1.

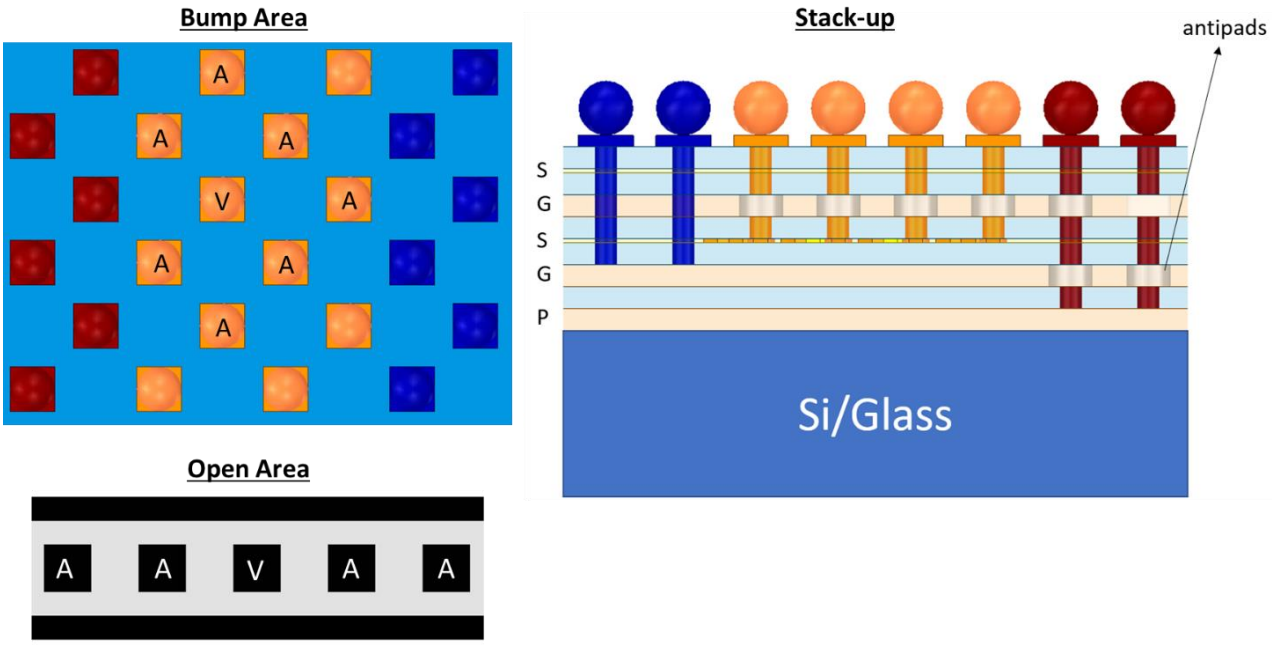


Figure 4-1: Bump area and channel routing open area (stripline configuration) [V stands for victim and A stands for aggressors]

Table 4-1: Geometric parameters for design of 2 µm RDL

	Silicon (SiO_2 RDL)	Glass (Polymer RDL)
Bump pitch	55 µm	55 µm
Bump diameter	22 µm	22 µm
Line Width	2 µm	2 µm
Line Spacing	2 µm	2 µm
Line Thickness	2 µm	2 µm
Dielectric Thickness	1 µm	1 µm
Signal Via Diameter	2 µm	2 µm
Signal Via Pad Diameter	5 µm	5 µm
Power/Ground Via Diameter	2 µm	2 µm
Chip-to-Chip Channel	6 mm	6 mm
Dielectrics	$\epsilon_r = 3.9, tan\delta = 0.002$ @20 GHz	$\epsilon_r = 2.4, tan\delta = 0.003$ @ 20 GHz

4.2 Results of design simulation

The extracted RLGC parameters are shown in Figure 4-2. As expected, the capacitance of polymer RDL due to the low dielectric constant of the polymer is significantly lower than silicon RDL. The capacitance between the lines/channels (marked as capacitive coupling as C23) is lower than the self-capacitance (C33) of the victim channel with respect to two ground planes of stripline configuration.

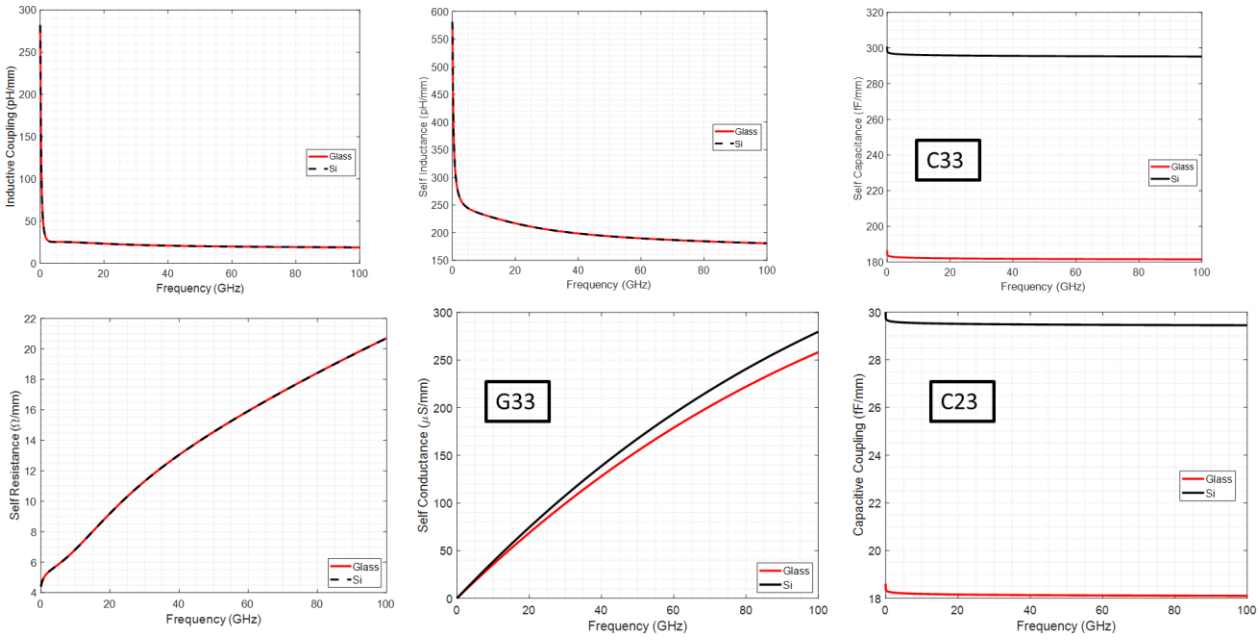


Figure 4-2: Extracted RLGC parameters for signal channels with geometric parameters defined in Table 4-1

The insertion loss of the signal for the glass polymer RDL is lower than silicon RDL due to this lower capacitive loss. The insertion loss, return loss, far-end and near-end crosstalk plots are shown in Figure 4-3.

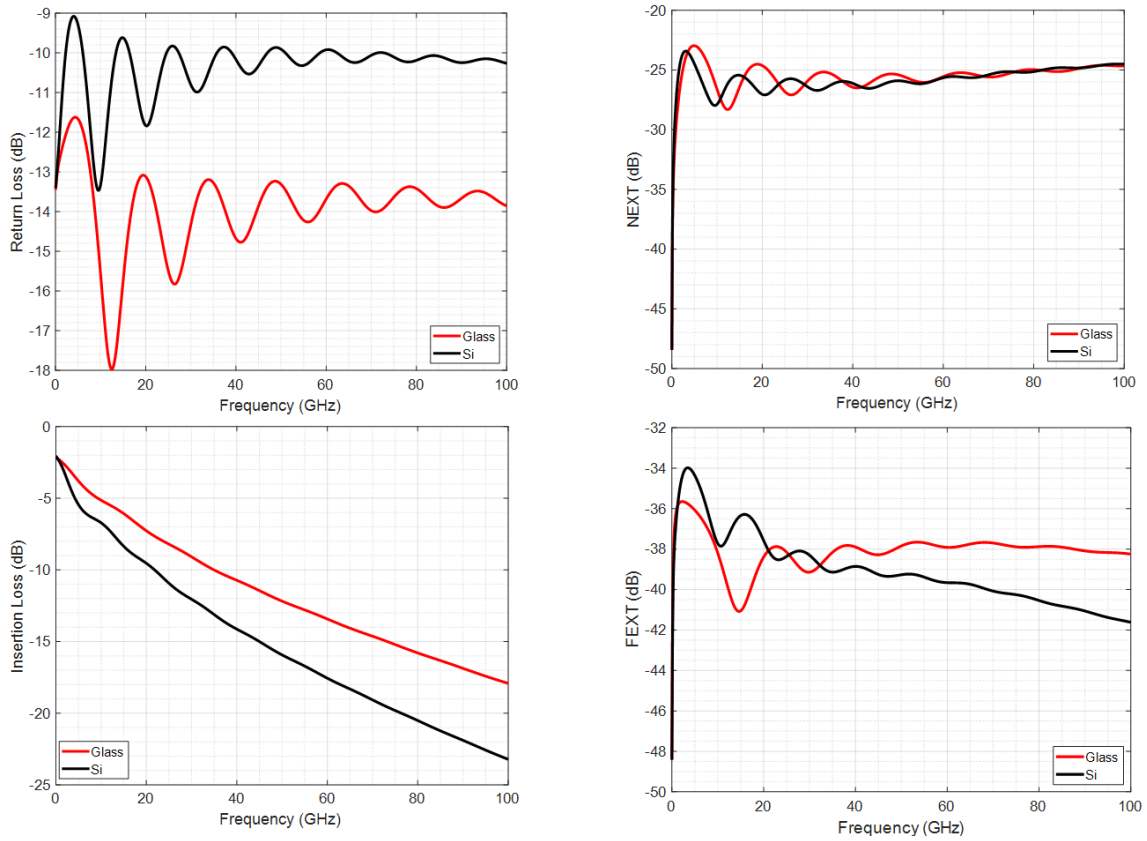


Figure 4-3: Insertion Loss, Return Loss, Near-End and Far-end crosstalk plots for glass polymer versus silicon SiO_2 RDL

The eye diagram comparisons for glass-based polymer RDL and silicon-based SiO_2 RDL along with the simulation settings used are shown in Figure 4-4. The simulations show that glass polymer RDL can handle higher signal data rates per channel. The product of eye height and eye width is a good estimate for determining the quality of the signal at the receiver side. Eye height and eye width of the channel are plotted for varying aspect ratios of copper line versus signal data rate as shown in Figure 4-5. In this study, the aspect ratios of the copper lines have been varied from 1 to 5 while keeping the dielectric thickness above and below the copper lines to be constant at 1 µm. Aspect ratio of 1 shows the best eye performance and the extracted RLGC parameters show that the rise in capacitance between the lines dominates over the reduced resistance. As frequency increases, the skin depth of copper lines decreases from 2 µm at 1 GHz to 0.92 µm at 5

GHz and finally to 0.65 µm at 10 GHz. Thus, at higher frequencies above 1 GHz, the flow of current is not through the entire channel of 2 µm width. Hence, the resistance does not proportionally decrease in a linear manner with the increasing aspect ratio. However, the capacitance is increasing linearly to the increasing aspect ratio. This is why, the rise in capacitance between the lines dominates over the reduced resistance.

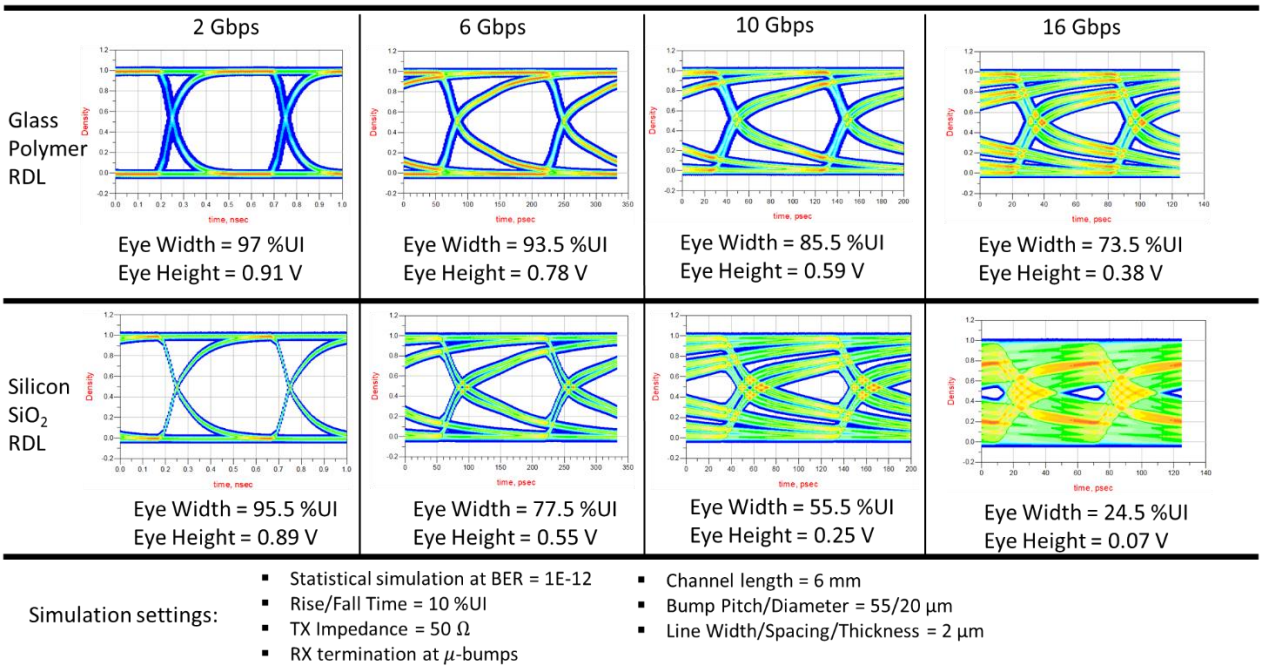


Figure 4-4: Eye Diagrams of glass polymer RDL versus silicon SiO_2 RDL for different signal data rates

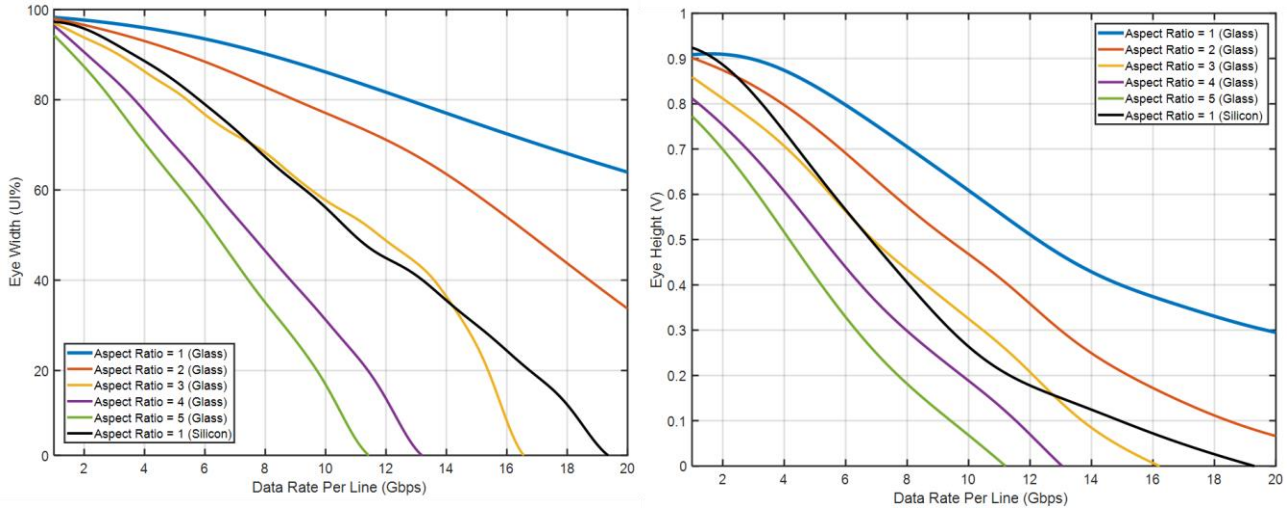


Figure 4-5: Eye width and eye height of glass polymer RDL versus signal data rate for varying aspect ratios of copper lines compared to silicon SiO_2 RDL with aspect ratio of 1

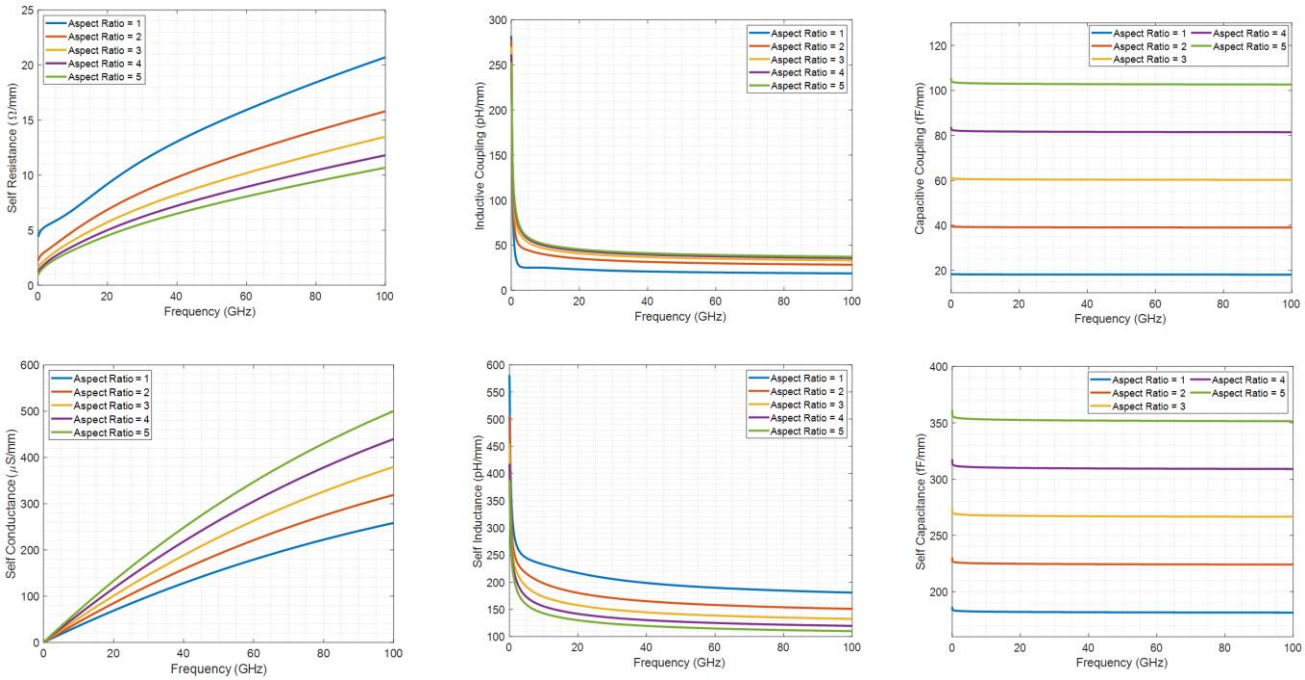


Figure 4-6: Extracted RLGC parameters for 2 μm width signal channel using glass polymer RDL with varying aspect ratios

For the geometry defined in Table 4-1, the line length was fixed at 6 mm and aspect ratio at one. The effect of changing line lengths with an aspect ratio of one is shown in Figure 4-7. At a

fixed signal data rate, the glass polymer RDL channel with 4 mm line length has similar performance to silicon SiO_2 RDL with 2 mm line length.

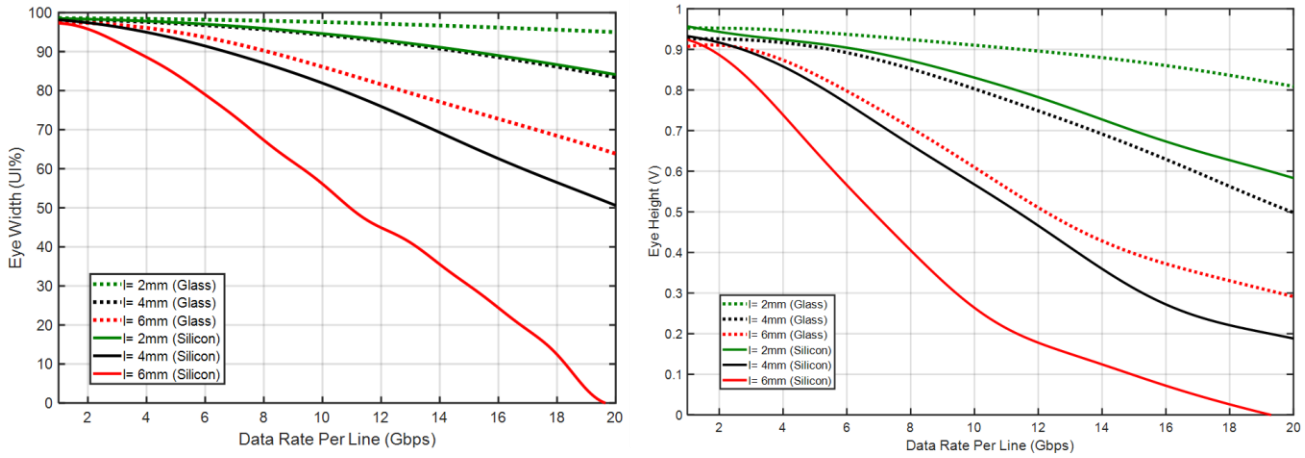


Figure 4-7: Effect of changing line lengths for silicon SiO_2 RDL versus glass polymer RDL at aspect ratio of 1

4.3 Design simulation for optimization of glass polymer RDL

The results in section 4.2 clearly indicate that glass polymer RDL can handle higher signal data rates than silicon polymer RDL. The lithography processes for glass polymer RDL can be used to scale to 1 µm line width which will be shown in section 5.1. At 5 GHz frequency, the skin depth of copper line is ~ 0.92 µm and the resistance will lower proportionally to increasing aspect ratios. The silicon BEOL RDL in 2.5D silicon interposers can handle 2 Gbps signal data rate (1 GHz frequency). In this research, the target is to increase the bandwidth by 5X for the same number of I/O wiring density. Thus, this section tries to optimize the signal performance at a fixed line length of 6 mm for: (A) Dielectric thickness and aspect ratio for a fixed 2 µm line width and 2 µm space between the lines and (B) Ideal line width, line space, aspect ratio and dielectric thickness for fixed pitch of (2*line width + line space = 6 µm). This fixed pitch ensures that the I/O wiring density is exactly the same as required for 2 µm line width and 2 µm space RDL. The simulations were done for both embedded microstrip and stripline configurations of transmission lines at 10

Gbps signal data rate. The optimized dielectric thickness for stripline configuration was around 3 µm. Stripline configuration with line width of 0.5 µm, line space of 5 µm and aspect ratio of 4.2 showed the best eye performance. Embedded microstrip line with a line width of 0.7 µm, line space of 4.6 µm and aspect ratio of 0.5 showed the second-best eye performance. The optimized dielectric thicknesses for embedded microstrip lines were 1.7 µm for top dielectric and 1 µm for bottom dielectric. For 2 µm line width and 2 µm space, the aspect ratio of 0.5 was found to have the best signal performance for both embedded microstrip and stripline configurations. The eye performance results are shown in Figure 4-8 for the optimized line geometry parameters versus signal data rate. At signal data rate of 10 Gbps, silicon BEOL RDL with stripline configuration at an aspect ratio of 1 showed eye width equal to 55 % UI and eye opening of 0.27 V. The optimized glass polymer RDL with stripline configuration (W =0.5, S =4, AR =4.2) shows eye width equal to 85 % UI and eye opening of 0.91 V. The high aspect ratio (~ 4) RDL with thick low D_k dielectrics (~ 3 µm) is processible with glass polymer RDL and hence, the bandwidth performance of glass polymer RDL is significantly higher than silicon BEOL RDL.

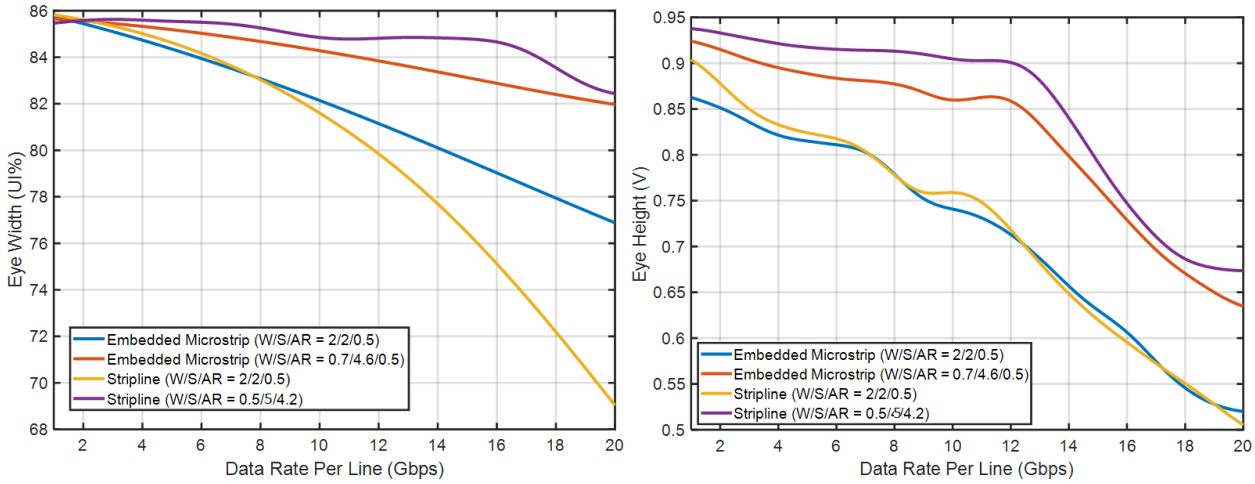


Figure 4-8: Optimized glass polymer RDL with embedded microstrip and stripline configurations (W= line width, S= line space and AR =aspect ratio)

The maximum signal data rate that can be passed through a channel is assumed to have an eye diagram with an eye width equal to ~ 80 % UI. With this assumption, silicon BEOL RDL with aspect ratio of 1 can handle 6 Gbps per channel (eye opening of 0.57 V) while glass polymer RDL with aspect ratio of 1 can handle 12 Gbps per channel (eye opening of 0.51 V). This is 2X bandwidth improvement with all other parameters kept constant. With the optimized glass polymer stripline RDL at a line width of 2 µm, space of 2 µm and an aspect ratio of 0.5, the signal channel can run at 12 Gbps with an eye opening of 0.72 V. For line width of 0.5 µm, space of 5 µm and aspect ratio of 4.2, the channel can run at signal data rates > 25 Gbps with eye opening of > 0.6V. The latency or rise time for a signal to reach 90 % of a step input 1 V signal was measured for silicon SiO_2 RDL and glass polymer RDL with 6 mm channel length. This value was 226 ps for silicon BEOL RDL and 72 ps for glass polymer RDL. Thus, design of glass polymer RDL shows that it can be scaled to 5X bandwidth than silicon BEOL RDL with 3X lower latency or delay. The jitter values for the eye diagram were calculated at 10 Gbps for optimized 2 µm line width, 2 µm line space and aspect ratio of 0.5 and shown in Table 4-2 below.

Table 4-2: Jitter calculations for silicon SiO_2 RDL versus glass polymer RDL at 10 Gbps

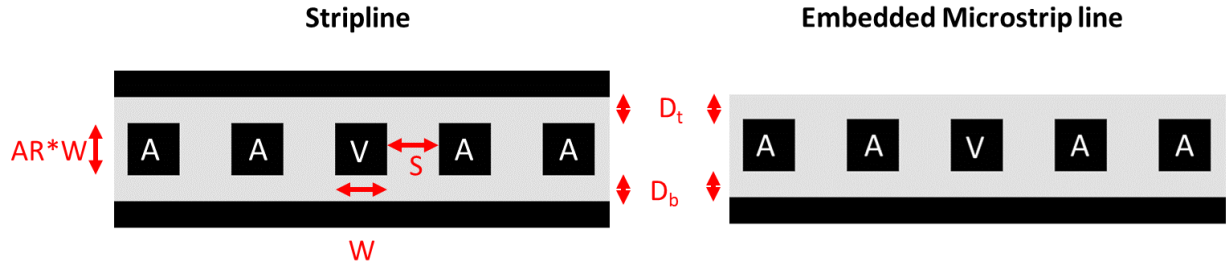
RDL	Line Width (W) in µm	Line Space (S) in µm	Aspect Ratio (AR)	Top Dielectric Thickness (D_t) in µm	Bottom Dielectric Thickness (D_b) in µm	Jitter (in ps) at 10 Gbps
Silicon SiO_2 (Stripline)	2	2	0.5	1	1	51 (51 % of UI)
Optimized Glass polymer RDL (Stripline)	2	2	0.5	3	3	12 (12 % of UI)
Optimized Glass polymer RDL (Embedded Microstrip line)	2	2	0.5	1.7	1	9.5 (9.5 % of UI)

4.4 Chapter 4 Summary

The design results of glass RDL with low dielectric constant polymer and silicon SiO_2 BEOL RDL clearly highlight the superior 5X bandwidth performance of glass polymer RDL at 3X lower latency than silicon BEOL RDL. The results are summarized in Table 4-3. The results highlight the need for development of high aspect ratio, fine pitch polymer RDL to achieve 5X higher bandwidth and 3X lower latency.

Table 4-3: Summary of design results of glass polymer RDL versus silicon SiO_2 RDL (The stripline and embedded microstrip line structures are shown with labels below the table)

RDL	Line Width (W) in µm	Line Space (S) in µm	Aspect Ratio (AR)	Top Dielectric Thickness (D_t) in µm	Bottom Dielectric Thickness (D_b) in µm	Signal data rate (Gbps) for eye width ~ 80 % UI	Eye opening (in Volts) for eye width ~ 80 % UI	Latency (ps) or rise time for signal to reach 90 % of a step input 1V signal
Silicon SiO_2 (Stripline)	2	2	1	1	1	6	0.57 @ 6 Gbps	226 ps
Glass polymer RDL (Stripline)	2	2	1	1	1	12	0.51 @ 12 Gbps	72 ps
Optimized Glass polymer RDL (Stripline)	2	2	0.5	3	3	12	0.72 @ 12 Gbps	
	0.5	5	4.2	3	3	> 25	> 0.6 @ 25 Gbps	
Optimized Glass polymer RDL (Embedded Microstrip line)	2	2	0.5	1.7	1	14	0.65 @ 14 Gbps	
	0.7	4.6	0.5	1.7	1	> 25	0.6 @ 25 Gbps	



CHAPTER 5. MATERIALS FOR 2 µm MULTI-LAYER POLYMER RDL

This chapter describes the photoresist materials required for fabrication of < 2 µm line width and space structures. It also includes the material design for polymer dielectrics required for two aspects: (A) Ideal mechanical properties like elastic modulus, % elongation to break, tensile strength and thermal properties like coefficient of thermal expansion (CTE) for fabrication of reliable < 5 µm diameter microvias and, (B) Excellent interfacial adhesion of titanium sputtered seed to smooth polymer dielectric.

5.1 Photoresist materials

Dry film photoresists (DFR) are easy to use compared to liquid spin-on resists for panel substrates. The uniform thickness of DFR across a large panel makes it an ideal candidate for high resolution lithography. High resolution, negative-tone DFR with thicknesses of 5 µm and 7 µm were used to enable very high-density wiring up to 3 µm line widths, leading to aspect ratios of 1-2. A novel i-line (365 nm), positive tone, chemically amplified (CA) dry film photoresist was developed for high-density fan-out and 2.5D interposer applications. The advantages of positive tone photoresists are higher resolution, higher yield due to less defects and they can be easily stripped because they do not undergo any crosslinking reactions like negative resists. Generally, CA photoresist is composed of hydrophobic polymer with a protecting group and a photo-acid generator (PAG). The PAG molecule generates acid during the UV exposure process (here 365 nm), and acid works as a catalyst for the deprotection reaction during post-exposure bake. Polymer in the exposed area (due to deprotection reaction) changes from hydrophobic to hydrophilic completely and is dissolved in the developer solution. As a result, CA photoresist enables better resolution than dry film negative tone photoresist which changes only molecular weight by crosslinking reaction during exposure. Other important advantages of CA photoresist are its ability

to achieve vertical walls and high aspect ratio structures. The CA photoresist system is designed for high sensitivity because the PAG molecules can act as catalyst as described above. The high sensitivity resist system allows to design the resist polymer with low i-line wavelength absorption. This allows the light to reach to the bottom of thick resists, enabling high aspect ratio structures while maintaining low exposure doses. Aspect ratios of up to 5-7 with 1 µm line width and space have been demonstrated in this study using CA positive dry film photoresist [53].

The patterning abilities of negative dry film resists, and liquid positive spin-on resists have been studied using a 0.12 NA (numerical aperture) projection stepper at a wavelength of 365 nm. The results are summarized in Table 5-1. These results are obtained by optimizing exposure doses and focus in the photoresist layer across the glass panel laminated with a polymer dielectric film sputtered with Ti-Cu seed. To pattern higher aspect ratio RDL (2-5) at 2 µm line widths or below, chemically amplified positive-tone dry film photoresist was used. The cross-section images of the RDL patterns at 2 µm line widths patterned using 15 µm thick resist are shown in Figure 5-1. The plated copper thickness is 10 µm. For 1 µm line width patterning, a 7 µm thick resist is used and plated to 5 µm thickness. This is shown in Figure 5-2. The minimum resolution achieved in this study is 1 µm line width at a space of 1.5 µm using a i-line projection stepper tool with 0.12 NA and depth of focus (DoF) of +/- 10 µm. With higher NA (NA= 0.24) tools being developed maintaining DoF of +/- 5 µm, the resolution could be scaled to < 1 µm line widths at aspect ratios of 4-5 [54].

Table 5-1: Feasibility studies of dry film negative resist and spin-on positive resist

	Dry Film P.R, Thickness, µm			Liquid P.R. Thickness, µm		
	10	*7*	*5*	*5*	*4*	*3*
L/S, µm	Aspect Ratio, σ			Aspect Ratio, σ		
5	2	1.4	1	1	0.8	0.6
4	2.5	1.8	1.25	1.3	1	0.75
3	3.3	2.3	1.67	1.7	1.3	1
2		3.5	2.5	2.5	2	1.5
1.5				3.3	2.7	2
1.2				4.2	3.3	2.5
1.0				5	4	3
0.9				5.6	4.4	3.3

Good Fair

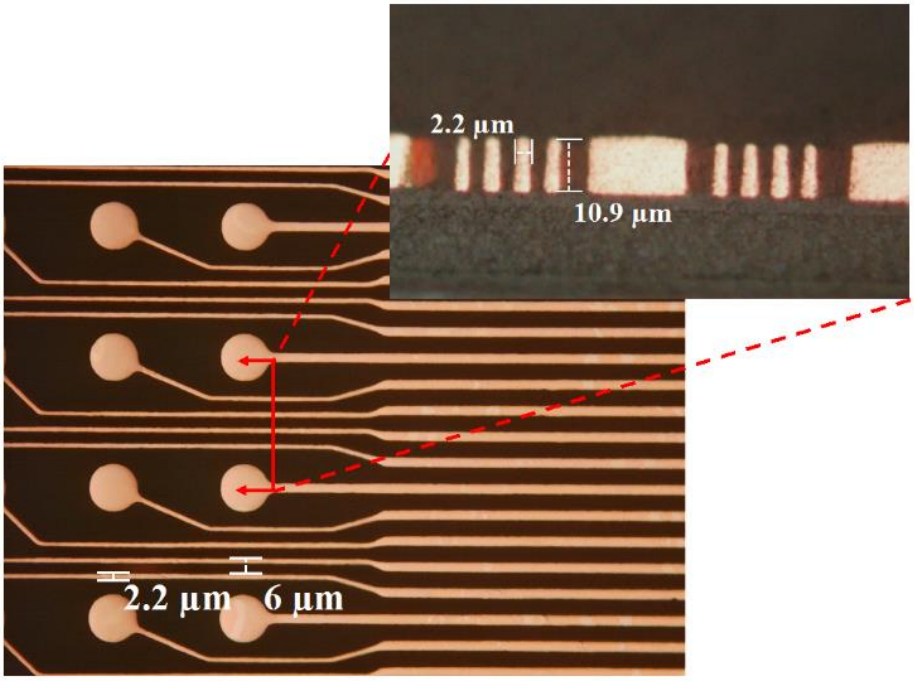


Figure 5-1: High aspect ratio (up to 5) plated copper RDL with 2 µm line width and 4 µm space using 15 µm thick chemically amplified positive photoresist

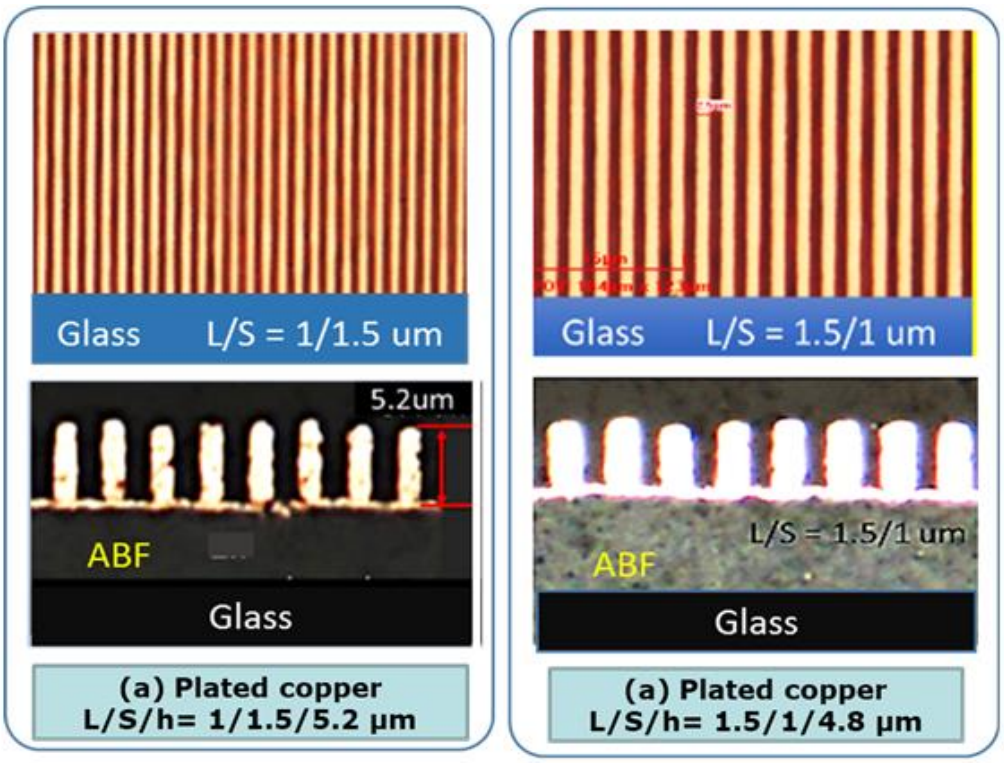


Figure 5-2: High aspect ratio (up to 5) plated copper RDL with 1-1.5 µm line width and 1-1.5 µm space using 7 µm thick chemically amplified positive photoresist [53]

5.2 Polymer dielectric materials

5.2.1 Material Design for fabrication of reliable < 5 µm diameter microvias

A typical high density, multi-layer RDL package substrate for high performance computing applications is shown in Figure 5-3 [[55], [56]]. There are three layers of stacked 10 µm diameter microvias in thin film, high density polymer RDL. This is the structure that will be used as a reference standard for thin film, high density polymer RDL. A three-layer stacked microvia polymer RDL structure is modeled using finite element analysis (FEA) with cross-section as shown in Figure 5-4. The variable geometric parameters for modeling microvia reliability are enlisted in Table 5-2. The material properties for the model are extremely critical for this study and are enlisted in Table 5-3.

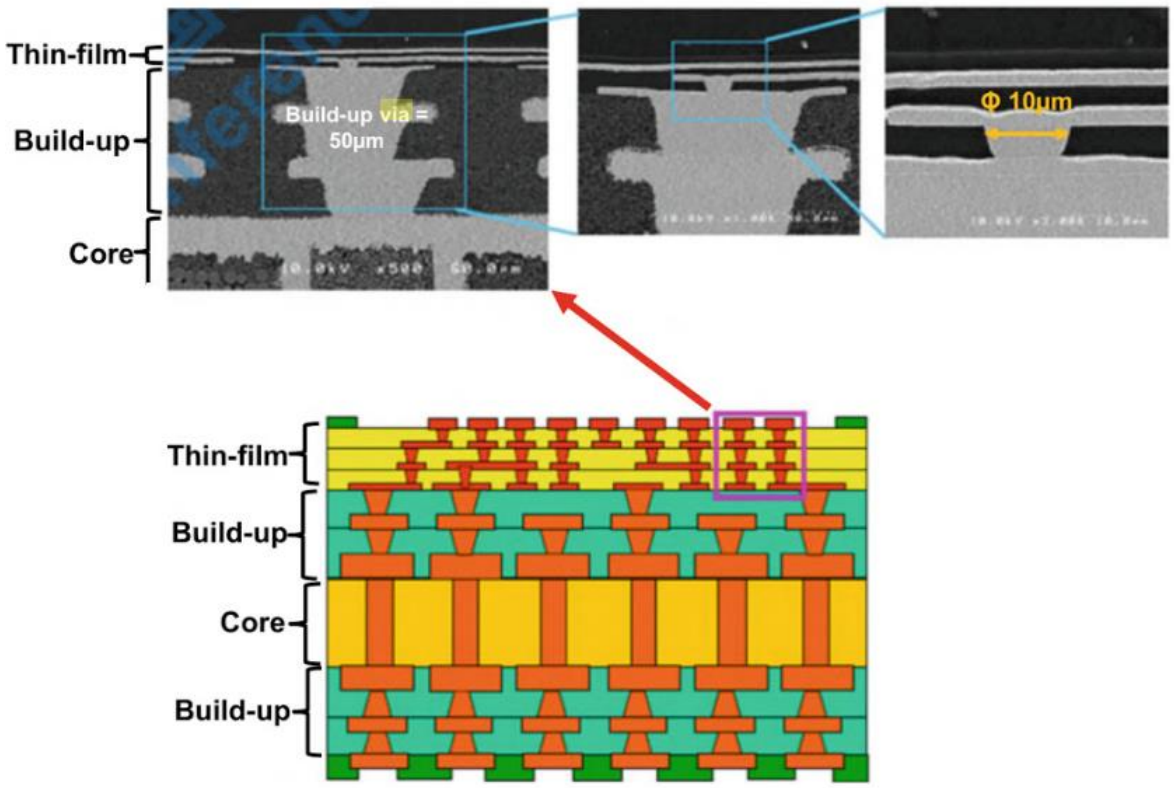


Figure 5-3: Shinko i-THOP RDL with three layers of stacked 10 µm diameter microvias in thin-film polymer RDL [55]

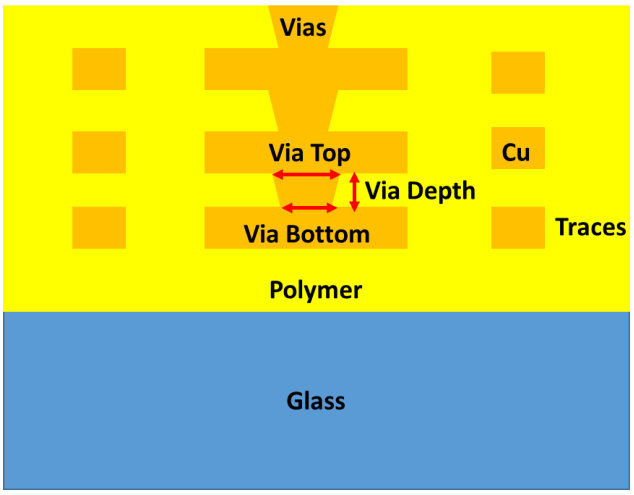


Figure 5-4: Three-layer stacked microvia model to determine stresses and strains in polymer and copper structures

Table 5-2: Parameters for modeling microvia reliability

No.#	Via Top (in µm)	Via Bottom (in µm)	Via Depth (in µm)	Aspect ratio of microvia (Via depth/Via Top)	Taper Angle (in degrees)	Copper trace Thickness (in µm)
A.	3	2	5	1.67	84.3	5
B.	3	2	2	0.67	75.9	2
C.	3	3	2	0.67	90	2
D.	4	2	2	0.5	63.4	2
E.	4	1.5	2	0.5	57.9	2

Table 5-3: Material Properties used for finite element model of microvia reliability

Material	Properties
Glass	Elastic Material Elastic Modulus: 77 GPa CTE: 3.3 ppm/K Poisson's Ratio: 0.34
Copper	Plastic material with Bilinear Kinematic Hardening Elastic modulus: 117 GPa CTE: 17 ppm/K Poisson's Ratio: 0.33 Rice's Hardening Rule for Kinematic Hardening with Yield Stress of 172.38 MPa and Tangent Modulus of 1034.2 MPa
Polymer dielectric	Elastic Material with Temperature Dependent Properties Modulus and CTE are function of temperatures Chemistries: PBO, PI, Epoxy with silica filler, BCB

The properties of polymer dielectric are dependent on the chemistry of the polymer resin and extracted from various literature sources. Dynamic mechanical analysis (DMA) was used to extract modulus versus temperature, tensile testing machine was used to extract tensile strength and % elongation to break properties versus temperature and thermo-mechanical analysis (TMA) was used to extract CTE versus temperature. The dependency of mechanical properties of polymer dielectrics with temperature considering examples of various grades of Ajinomoto build-up film

(ABF) (epoxy-silica filler-based dielectrics) are shown in Figure 5-5. GZ-20 represents epoxy polymer dielectric with high silica filler content (50 wt. %) and GX-13 represents epoxy polymer dielectric with moderate silica filler content (38 wt.%) [57]. The CTE dependency with temperature for epoxy-silica filler dielectric is shown in Figure 5-6. Based on these data sets, this research identifies five class of polymers to evaluate the ideal properties required for material design for fabrication of reliable microvias below 5 µm diameter. This is shown in Table 5-4. Some of the properties in the table are assumed based on the property trends of polymer dielectrics as shown in Figure 5-5 and Figure 5-6.

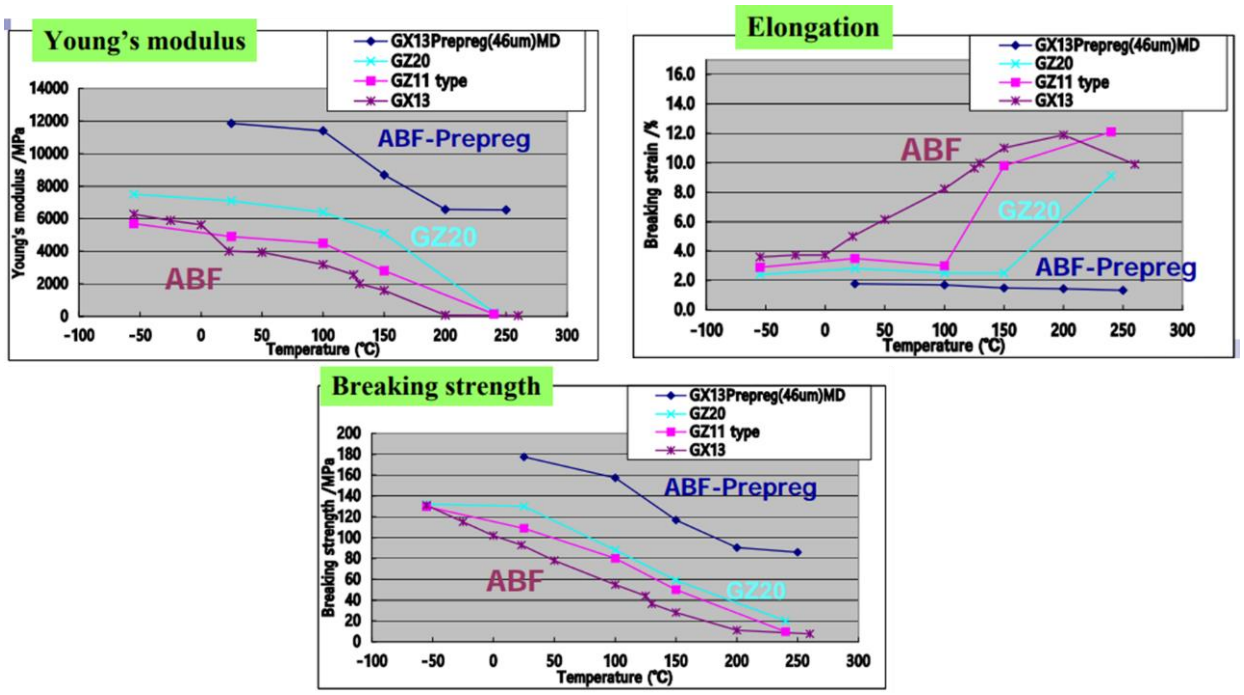


Figure 5-5: Variation in mechanical properties of ABF dielectrics versus temperature [57]

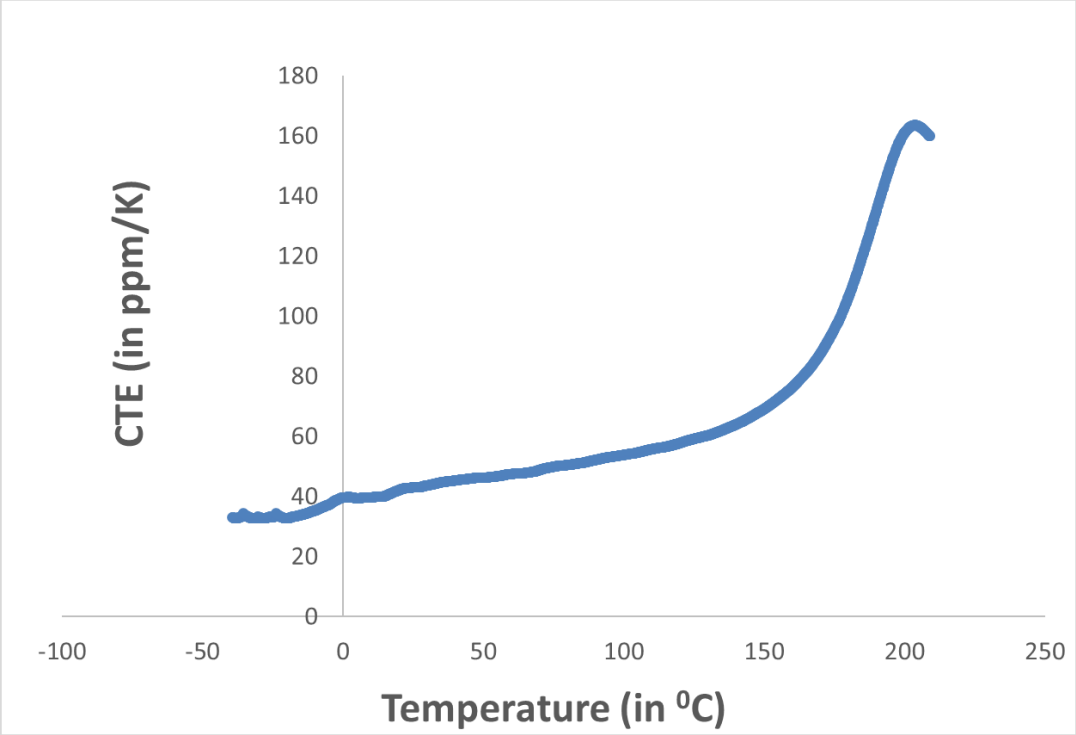


Figure 5-6: Variation in CTE of a typical epoxy-silica filled polymer dielectric versus temperature (Room temperature CTE is 42 ppm/K)

Table 5-4: Material properties of polymer dielectrics for evaluating microvia reliability

Material Class	Elastic Modulus (GPa)			Instantaneous CTE (ppm/K)			Tensile Strength (MPa)			Elongation to Break (%)		
	-55^{0}C	25^{0}C	125^{0}C	-55^{0}C	25^{0}C	125^{0}C	-55^{0}C	25^{0}C	125^{0}C	-55^{0}C	25^{0}C	125^{0}C
Epoxy with 38% silica filler	6.3	4.0	2.0	33	43	62	130	93	40	4.0	5.0	10.0
Epoxy with 50% silica filler	7.8	7.1	5.8	24	28	54	135	130	75	2.1	2.8	2.5
BCB	4.0	3.0	2.2	33	42	60	95	87	> 50	6-7	8-9	> 10
Polyimide (PI) (high cure temp)	4.5	3.4	2.5	30	35	55	230	200	> 100	> 20	45	>50
Polybenzoxazole (PBO)	3.0	2.2	1.5	52	60	80	200	170	> 100	> 10	100	> 100

A finite element model is used to simulate the three-layer stacked microvia structure shown in Figure 5-4 using the properties of polymer dielectrics shown in Table 5-4. The set of geometric parameters for the model is shown in Table 5-2. The load condition includes thermal cycling from -55 ^{0}C to 125 ^{0}C. There are two aspects of reliability that are being considered:

(A) Total strain range (TSR) in fully-filled copper microvia structure to predict cycles to failure using fatigue models for copper as described in section 2.3 and equation (2-1). The difference in Von Mises total mechanical strain at -55 ^{0}C and 125 ^{0}C will be the TSR value for copper. This is shown as an example in Figure 5-7.

(B) Von Mises total mechanical strain and Von Mises equivalent stress in polymer dielectric surrounding the microvia. If the total strain exceeds the % elongation to break or the total stress exceeds the tensile stress of polymer dielectric enlisted in Table 5-3, the polymer is bound to crack. An example is shown in Figure 5-8.

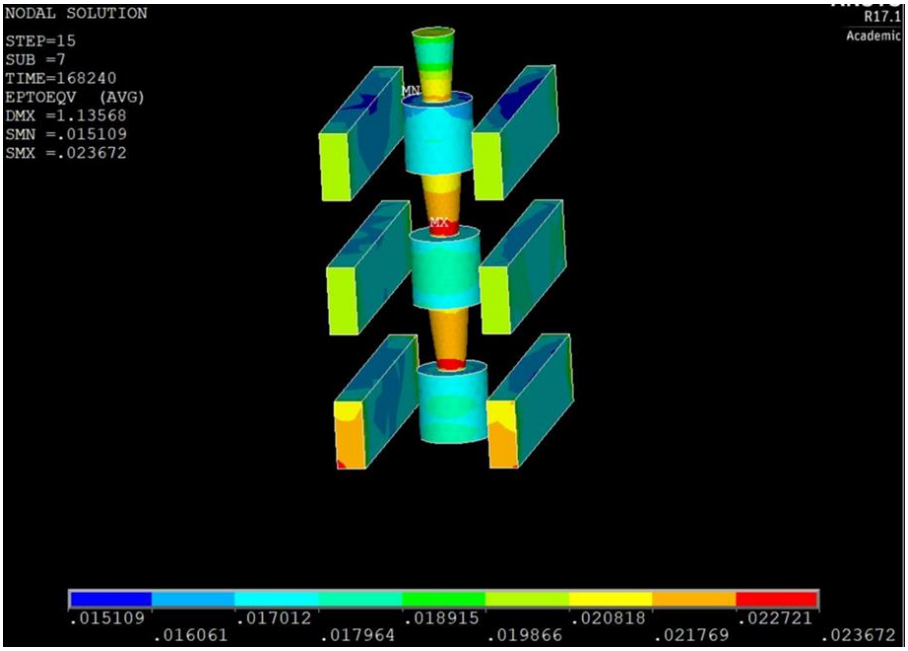


Figure 5-7: Von Mises Total Mechanical Strain of 0.0236 in copper at -55 ^{0}C

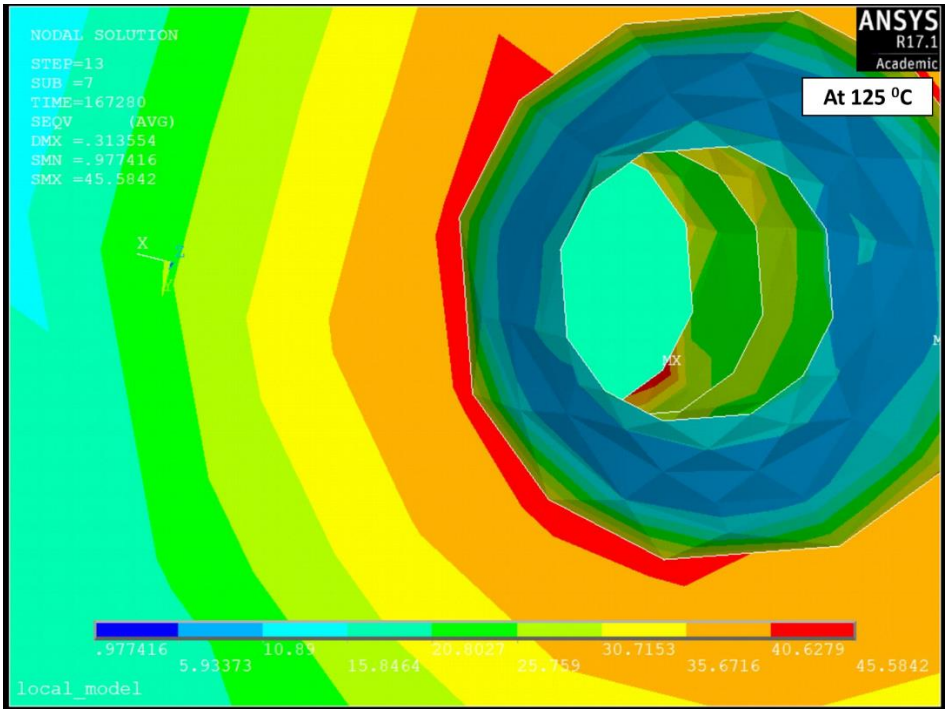


Figure 5-8: Von Mises Equivalent stress of 45.6 MPa in polymer at 125 ^{0}C

The results are summarized in a tabular form for each dielectric set. The first set of data for epoxy polymer dielectric with moderate (38 wt.%) silica filler content is shown in Table 5-5. The data clearly suggests that higher aspect ratio > 1 (case A) is not recommended for small microvias. For cases (B) and (C), the higher taper angle in case B tends to increase the TSR in copper. Hence, case (B) falls well below recommended 1000 cycles to failure criteria. For case (C) with the perfect 90^0 taper angle, the TSR in copper is minimum and the structure can reliably pass 7000 cycles to failure. The stress in polymer at -55 ^{0}C (111 MPa) is well below the tensile strength of polymer (130 MPa) but 54 MPa stress in polymer at 125 ^{0}C exceeds the tensile strength of polymer (40 MPa). For cases (D) and (E), the polymer dielectric is not suited for recommended 1000 cycles to failure. Thus, such a dielectric is suited only for close to 90^0 taper angle microvias and a higher tensile strength is preferred at 125 ^{0}C.

Table 5-5: Stress and strain data for different microvia geometries with epoxy polymer dielectric containing moderate (38 wt.%) silica filler content

No. # (Refer Table 5.2)	Von Mises Total Mechanical Strain in copper		TSR	Predicted Cycles to Failure using Engelmaier's model	Von Mises Total Mechanical Strain in polymer		Von Mises stress in polymer (MPa)	
	-55^{0}C	125^{0}C			-55^{0}C	125^{0}C	-55^{0}C	125^{0}C
A.	0.018	0.005	0.013	715	0.019	0.012	160	60
B.	0.017	0.005	0.012	875	0.018	0.014	148	89
C.	0.012	0.006	0.006	7000	0.018	0.013	111	54
D.	0.021	0.006	0.015	500	0.017	0.011	109	55
E.	0.027	0.007	0.02	250	0.05	0.015	144	54

The first set of data for epoxy polymer dielectric with high (50 wt.%) silica filler content is shown in Table 5-6. The data clearly suggests that higher aspect ratio > 1 (case A) is again not recommended for small microvias. This case will not be considered for the simulations of other polymer dielectrics. It is not recommended to fabricate < 5 µm diameter microvias above aspect ratio of 1. For cases (B)-(E), the TSR in copper is minimum and the structure can reliably pass > 20000 cycles to failure. Thus, low CTE of polymer dielectric (as close to copper) is preferred for high reliability of copper in microvia structure. For smaller taper angles (cases (D) and (E)), the stress in polymer at -55 ^{0}C is a big concern, approaching the tensile strength of polymer (135 MPa). In addition to this, for case (E), the strain in polymer at -55 ^{0}C (2.8 %) is exceeding the % elongation to break of polymer (2.1 %). Thus, for such low CTE polymer dielectrics, high % elongation to break and high tensile strength properties are recommended for fabrication of reliable microvias below 5 µm diameter. The fatigue response behavior of polyimide thin film under cyclic loading has been studied by Yu-Chen Chang et.al. for different stress values [58]. As shown in Figure 5-9, the results indicate that there is an elongation increment of 3-5 % under typical 110-130 MPa constant fatigue stress in polyimide dielectric for N > 5000 cycles. Assuming these

results for epoxy dielectric as well, the ideal low CTE polymer dielectric should have > 6-7 % elongation to break at -55 ^{0}C, which translates to > 8-9 % elongation to break at 25 ^{0}C and tensile strength > 150 MPa at -55 ^{0}C, which translates to tensile strength > 160 MPa at 25 ^{0}C.

Table 5-6: Stress and strain data for different microvia geometries with epoxy polymer dielectric containing high (50 wt.%) silica filler content

No. # (Refer Table 5.2)	Von Mises Total Mechanical Strain in copper		TSR	Predicted Cycles to Failure using Engelmaier's model	Von Mises Total Mechanical Strain in polymer		Von Mises stress in polymer (MPa)	
	-55^{0}C	125^{0}C			-55^{0}C	125^{0}C	-55^{0}C	125^{0}C
A.	0.02	0.009	0.011	1050	0.025	0.009	140	90
B.	0.009	0.005	0.004	> 20000	0.012	0.008	119	78
C.	0.008	0.007	0.001	> 20000	0.014	0.007	95	62
D.	0.008	0.004	0.004	> 20000	0.017	0.011	130	86
E.	0.009	0.005	0.004	> 20000	0.028	0.012	143	83

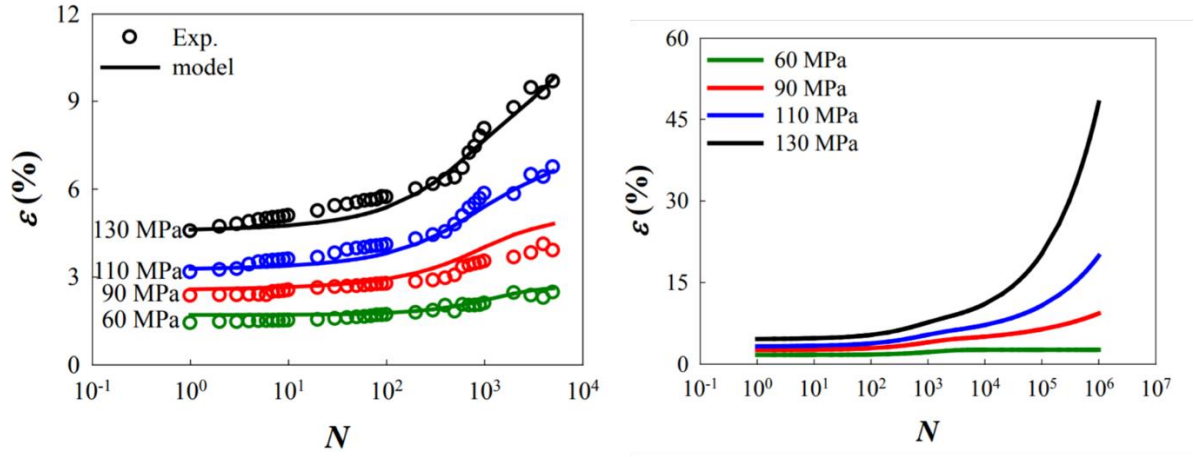


Figure 5-9: Evolution of strain in polyimide thin film dielectric under stress-controlled cyclic fatigue loading [58]

The results with BCB were similar to the one shown in Table 5-5 and clearly indicate the need for a higher tensile strength material to prevent polymer cracking. The results with high cure temperature polyimide are summarized in Table 5-7 and indicate that 90^0 taper angle microvias as

in case (C) or lower aspect ratio microvia structures as in cases (D) and (E) are preferable for lower TSR in copper and higher cycles to failure. The polymer stress is increasing with higher taper angle for a fixed aspect ratio. With high tensile strength and high % elongation to break properties of polyimide, the material is very reliable to cracking failures. However, the biggest challenge is the high cure temperature of this polyimide (> 300 ^{0}C) and the moisture absorption (> 1.5 wt. %) for electrochemical migration reliability of fine line and space RDL. The results with high CTE polymers like PBO as shown in Table 5-8 clearly indicate that such dielectrics are not suited for reliability of small microvia structures in terms of number of cycles to failure.

Table 5-7: Stress and strain data for different microvia geometries with high cure temperature polyimide (PI)

No. # (Refer Table 5.2)	Von Mises Total Mechanical Strain in copper		TSR	Predicted Cycles to Failure using Engelmaier's model	Von Mises Total Mechanical Strain in polymer		Von Mises stress in polymer (MPa)	
	-55^{0}C	125^{0}C			-55^{0}C	125^{0}C	-55^{0}C	125^{0}C
B.	0.016	0.006	0.0099	1470	0.008	0.004	102	33
C.	0.011	0.005	0.0055	10000	0.017	0.009	42	22
D.	0.015	0.006	0.0089	1900	0.03	0.009	122	30
E.	0.017	0.006	0.0116	1000	0.04	0.008	135	35

Table 5-8: Stress and strain data for different microvia geometries with high CTE polybenzoxazole (PBO)

No. # (Refer Table 5.2)	Von Mises Total Mechanical Strain in copper		TSR	Predicted Cycles to Failure using Engelmaier's model	Von Mises Total Mechanical Strain in polymer		Von Mises stress in polymer (MPa)	
	-55^{0}C	125^{0}C			-55^{0}C	125^{0}C	-55^{0}C	125^{0}C
B.	0.028	0.005	0.022	210	0.049	0.013	128	33.6
C.	0.019	0.003	0.016	425	0.022	0.01	56.3	18.8
D.	0.028	0.005	0.023	190	0.056	0.011	145	27.2
E.	0.036	0.009	0.027	140	0.061	0.013	160	33.2

To benchmark with the current Shinko i-THOP RDL, the model was simulated using the geometric parameters shown in Figure 5-4. The properties of polymer dielectric at room temperature were extracted from [56] and extended to -55 ^{0}C and 125 ^{0}C temperatures using the trends of polymer dielectric properties observed in Table 5-4. The results are shown in Table 5-9 and indicate the excellent reliability of microvia stacked structure in Shinko i-THOP RDL. The reliability of the microvia structure is excellent in all three aspects:

(i) Cycles to failure for fully-filled copper microvia (> 2500 cycles)

(ii) Stress in polymer dielectric is 91 MPa at -55 ^{0}C while the tensile strength of such a polymer dielectric at room temperature is > 95 MPa, which suggests tensile strength of polymer dielectric at -55 ^{0}C is > 120 MPa, well above the observed stress of 90 MPa.

(iii) Strain in polymer dielectric is 2.6 % at -55 ^{0}C while the % elongation to break of polymer dielectric at room temperature is 6.5 %, which suggests % elongation to break of polymer dielectric at -55 ^{0}C is ~ 5 %. From Figure 5-9, under a stress of 90 MPa and 2.6 % elongation, the polymer is elongated to ~ 5% and prone to cracking only after 5000 fatigue cycles.

Table 5-9: Stress and strain data for Shinko i-THOP RDL

Shinko i-THOP RDL	Von Mises Total Mechanical Strain in copper		TSR	Predicted Cycles to Failure using Engelmaier's model	Von Mises Total Mechanical Strain in polymer		Von Mises stress in polymer (MPa)	
	-55^{0}C	125^{0}C			-55^{0}C	125^{0}C	-55^{0}C	125^{0}C
10 µm via top 7.5 µm via bottom 3 µm via depth	0.013	0.005	0.008	2700	0.026	0.011	91	38

With these results, the properties of ideal polymer dielectric for fabrication of reliable three-layer stacked microvias are proposed in Table 5-10.

Table 5-10: Properties of ideal polymer dielectric for fabrication of reliable three-layer stacked microvias with 2 µm diameter

Material Class	Elastic Modulus (GPa)			Instantaneous CTE (ppm/K)			Tensile Strength (MPa)			Elongation to Break (%)		
	-55^{0}C	25^{0}C	125^{0}C	-55^{0}C	25^{0}C	125^{0}C	-55^{0}C	25^{0}C	125^{0}C	-55^{0}C	25^{0}C	125^{0}C
Ideal low cure temp, low moisture absorption PI like dielectric	4.5	3.4	2.5	30	35	55	> 150	> 120	> 60	> 7	> 10	> 10

A novel photosensitive epoxy dielectric material with nano-silica filler was developed with a room temperature CTE of 35 ppm/K and modulus of 4 GPa. The maximum elongation that could be achieved was 6 % at 25 ^{0}C and the water absorption was 0.8 wt. %. The material has a combination of properties with a low CTE corresponding to that of high cure temperature polyimide and the modulus corresponding to that of epoxy with 38 wt.% silica filler. The tensile strength is similar to the epoxy with 38 wt.% silica filler of 95 MPa at 25 ^{0}C and 130 MPa at -55 ^{0}C. The % elongation to break is slightly higher than the epoxy equivalent. The low cure temperature of the epoxy at 180 ^{0}C for 1 hour makes it an attractive candidate for low temperature processing. With these properties, it is necessary to have a tighter process control of maintaining taper angles between 70^0-90^0 during microvia fabrication.

5.2.2 Material Design for superior interfacial adhesion of titanium sputtered seed to smooth polymer dielectric

To predict the chemical properties of dielectric (in this case, interfacial adhesion with metal seed) required for reliable high aspect ratio fabrication of 2 µm RDL, the stresses due to deposition of conductor structures need to be calculated. The residual stress at the interface of a bilayer thin film and substrate system is composed significantly of two components as shown below [35]:

$$\sigma_{residual} = \sigma_{intrinsic} + \sigma_{thermal} \quad \textbf{Eq. (5-1)}$$

The intrinsic stresses are due to the metal deposition processes such as sputtering and electroplating. These are dependent on individual fabrication processes and are characterized using a BowOptic 208- Wafer Stress Measurement tool. The tool measures the stress by calculating the change in the radius of curvature of a silicon wafer after the deposition of a thin film. The thermal stresses are due to the mismatch in CTE between the thin film and substrate during the cooling process from high temperature. The thermal stresses are predicted from the below equation (5-2). In the equation below, α_F and α_S are the CTE of the film and substrate respectively, while E and υ denote the elastic modulus and Poisson's ratio of the thin film respectively. The factor ($T-T_{dep}$) denote the temperature difference. In our experiments, T is the room temperature while T_{dep} is the highest temperature to which the substrate is exposed. Thus, cooling a plated copper layer on silicon substrate from 150 ^{0}C to 25 ^{0}C would be negative ($T-T_{dep}$) and thereby, results in a positive tensile stress.

$$\sigma_T = -E * (\alpha_F - \alpha_S) * \frac{(T - T_{dep})}{1-\nu} \quad \textbf{Eq. (5-2)}$$

The total residual stresses from equations (5-1) and (5-2) indicate that the CTE of polymer dielectrics alter the total stress at polymer-copper interfaces. Thus, higher CTE dielectrics will require a higher peel strength than that required for low CTE dielectrics. The stresses are simulated for the polymer-copper interface using the same structure shown in Figure 5-4. The stresses in Z-direction at -55 ^{0}C and 125 ^{0}C, perpendicular to the cross-sectional area of polymer-copper interface, are used to predict the stress generated in polymer-copper interfaces for the areas surrounding 2 µm width copper lines. Equation (2-2) in section 2.3 is used to determine the required peel strength from the polymer-copper interfacial stress in different polymer dielectrics

to reliably fabricate 2 µm RDL at high aspect ratios. A typical result is shown in Figure 5-10. Table 5-11 summarizes the peel strength required for high aspect ratio 2 µm RDL using low CTE and high CTE polymer dielectrics. A 2 µm RDL with 5-10 µm thickness is typical for high CTE photosensitive dielectric-based embedded trench RDL with via-in-line structures. For such structures, high peel strength of 0.74 kgf/cm will be required to pass thermal cycling reliability at -55 ^{0}C. This model does not include any intrinsic stresses since the measured values were negligible after the copper annealing process. The intrinsic stresses for sputtered metal thin films and electroplated thick copper films were measured by deposition of films on a 1 mm thick silicon wafer and measuring the bow of the wafer before and after deposition. The results for measured intrinsic stresses are summarized in Table 5-12. From the results in Table 5-11, there is a need to develop dielectrics with enhanced peel strength between copper and polymer for high aspect ratio RDL.

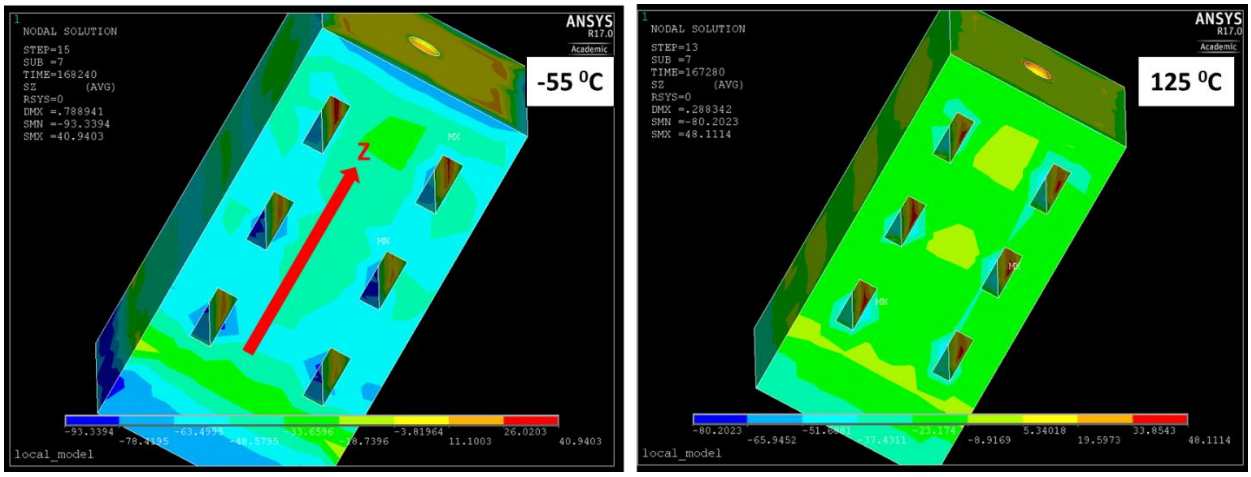


Figure 5-10: Stresses in Z-direction (in MPa) at the polymer-copper interface at -55 ^{0}C and 125 ^{0}C

Table 5-11: Required peel strength for high aspect ratio 2 µm RDL

Material	Interfacial Stress in Z-direction (in MPa) (Compressive (-) and Tensile (+))		Thickness of 2 µm width copper line (in µm)	Required Peel Strength (in kgf/cm) (Equation 2-2)
	-55^{0}C	125^{0}C		
Low CTE dielectric (Epoxy with 50 wt.% silica)	**-42**	-26	**2**	**0.084**
	-47	-29	**5**	**0.235**
	-48	-32	**10**	**0.480**
High CTE dielectric (PBO)	**-65**	-31	**2**	**0.130**
	-69	-29	**5**	**0.345**
	-74	-47	**10**	**0.740**

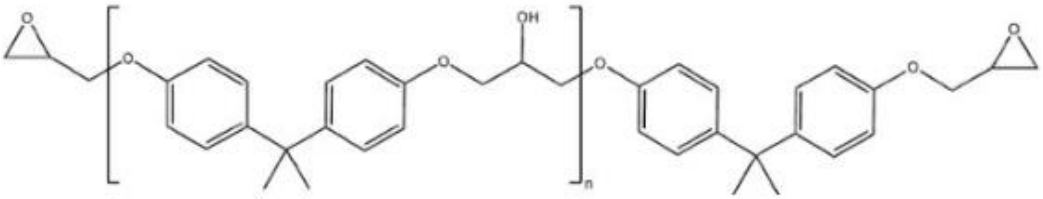
Table 5-12: Calculation of Interfacial Residual Stresses using a Wafer Bow-Optic Tool

Material	Stress Tensile (+) and Compressive (-)
Intrinsic stress of Ti seed layer (50 nm thick)	- 400 MPa
Intrinsic stress of Cu seed layer (200 nm thick)	+ 200 MPa
Net intrinsic stress after copper electroplating (3-8 µm thick) on sputtered Ti-Cu seed (Before Annealing)	-15 to -50 MPa
Net intrinsic stress after copper electroplating (3-8 µm thick) on sputtered Ti-Cu seed (After Annealing)	-10 to +10 MPa

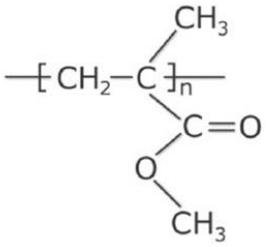
Three different dielectrics are chosen with two different chemistries to understand the bonding mechanism of titanium seed and polymer dielectric. The representative chemical structures of these polymer dielectrics are shown in Figure 5-11. Titanium is known to have a great affinity with oxygen and the chosen polymer dielectrics have almost similar amounts of C-O moieties as measured by X-ray photoelectron spectroscopy (XPS) and shown in Figure 5-12. The properties of these dielectrics are summarized in Table 5-13.

Table 5-13: Properties of dielectrics for characterizing interfacial adhesion

Parameters	Dielectric A	Dielectric B	Dielectric C
Material	Non-photosensitive epoxy	Photosensitive epoxy	Photosensitive acrylic
Coefficient of Thermal Expansion (CTE) (in ppm/K from 25-150 ^{0}C)	39	45	60
% Amount of C-C and C-O bond groups	74 % and 26 %	61 % and 39 %	57 % and 30 %
% Amount of C=O bond groups	-	-	13 %



(A)



(B)

Figure 5-11: Representative chemical structures of (A) Epoxy resin (B) Acrylic resin

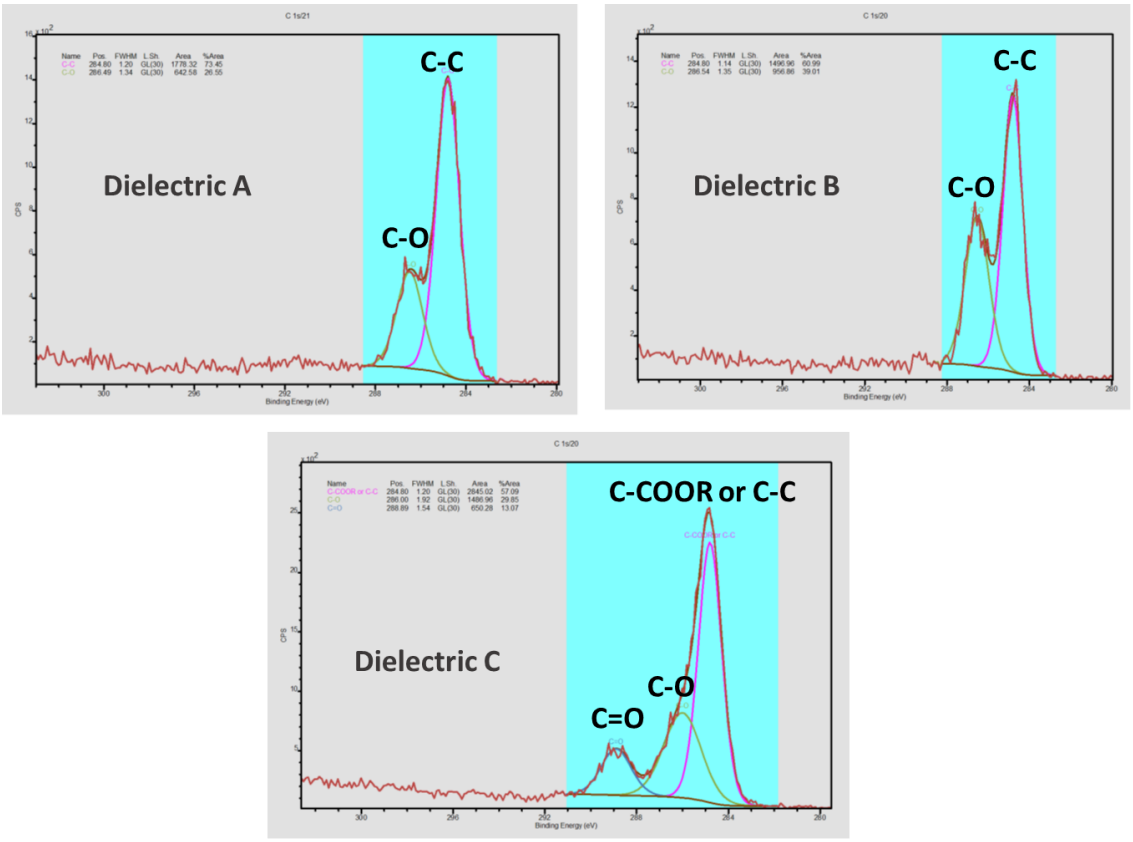
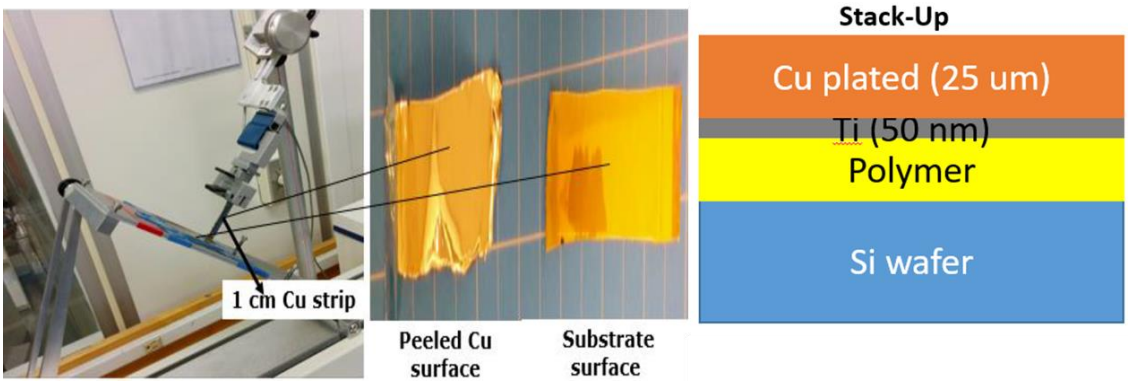


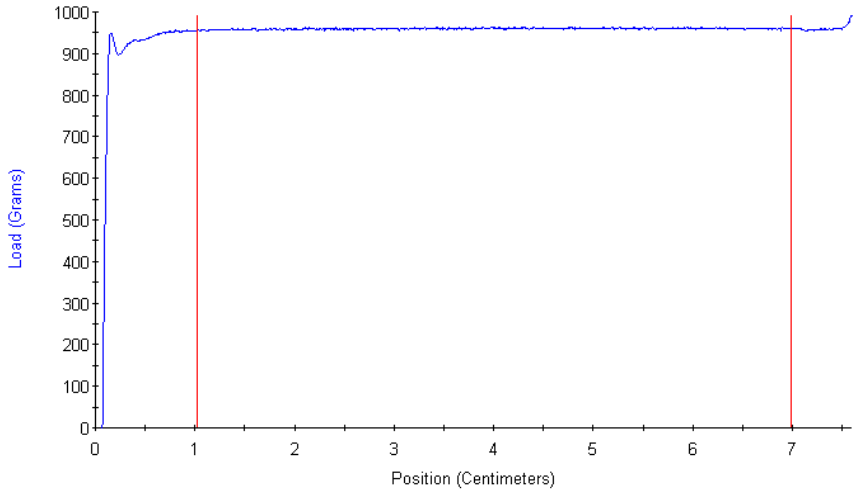
Figure 5-12: X-ray photoelectron spectroscopy (XPS) surface scans of polymer dielectrics A, B and C

The peel strength test is a quantitative way of characterizing metal-polymer adhesion. There are two important parameters that control interfacial adhesion of sputtered metal seed and polymer dielectric: (A) Intrinsic stress of sputtered titanium thin films and, (B) Strength of chemical bond formed between sputtered titanium film and polymer dielectric. A blank silicon wafer of 500 µm thickness is laminated with 5 µm thick dry film dielectric and cured. The polymer laminated wafers are degassed in a N_2 oven at 150 ^{0}C for 30 mins and later treated using Inductively Coupled Plasma (ICP) Argon etch equivalent to 20 nm of SiO_2 etch. The change in nano-roughness before and after Argon ICP etch was shown to be a factor of 3X. The dielectric average roughness (R_a) of all the three dielectrics were below 40 nm before argon ICP etch and increased to ~ 100 nm after argon ICP etch. The polymer dielectric laminated wafer sample is then

DC sputtered with 50 nm titanium barrier and 200 nm copper seed. The seed layer coated samples are annealed at 150 ^{0}C for 30 mins at a rate of 5 ^{0}C/min and cooled down to room temperature overnight at a rate of 1-2 ^{0}C/min. The blanket seed samples are electroplated to 25 μm thickness and annealed again at 190 ^{0}C for 1.5 hours at a rate of 5 ^{0}C/min and cooled down to room temperature overnight at a rate of 1-2 ^{0}C/min. The plated sample is peeled at a 90^0 angle at the rate of 12 inches/min. A typical peel test set-up and result are shown in Figure 5-13, where the Y-axis represents the force in grams required to peel a 1 cm wide strip over a minimum length of 5 cm. The effect of varying intrinsic stress of sputtered titanium seed thin film is shown in Figure 5-14. The high compressive intrinsic stress in sputtered titanium film results from more metal atoms being jammed into interstitial lattice sites and this can lead to a higher number of titanium-polymer bonds at the interface [59]. This can be a possible explanation for the observed higher peel strength as compressive intrinsic stress of sputtered titanium thin film increases.



(A)



(B)

Figure 5-13: (A) Set-up for characterization of 90-degree peel strength tests and (B) A typical peel test result

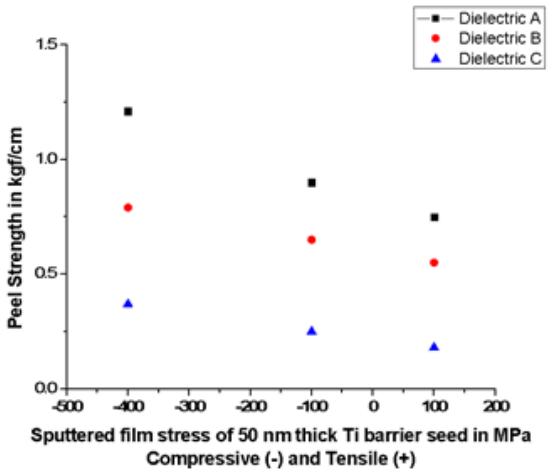


Figure 5-14: Effect of sputtered film stress of 50 nm thick titanium barrier seed in MPa on the peel strength with different polymer dielectrics

To understand the effect of dielectric chemistry, the samples were sputtered with titanium seed of -400 MPa intrinsic stress and electroplated and annealed for peel strength measurements. The samples were subjected to two different reliability tests: (A) Liquid-to-liquid thermal shock cycling and (B) Unbiased pressure cooker test. Prior to exposing to the reliability tests, the samples were pre-conditioned in three steps: (A) Sample baking at 125^0C for 24 hours (B) Moisture sensitivity level-3 conditioning at 60^0C, 60% RH for 40 hours and (C) Three solder reflow cycles with a peak temperature of 260^0C. The thermal shock cycling reliability test induces thermo-mechanical stress-based delamination at metal-polymer interfaces. Each cycle comprised of a dwell time of 5 mins at 125^0C and another 5 mins at -55^0C. The transfer time from one bath to the other bath was 10 seconds. The samples were then exposed to 1000 thermal shock cycles. The unbiased pressure cooker test can cause moisture-induced degradation of metal-polymer interfaces. The samples were also separately subjected to unbiased pressure cooker test at 130^0C, 85% RH for 100 hours. The average of three peel strengths of samples in kgf/cm before and after reliability tests are summarized in Figure 5-15.

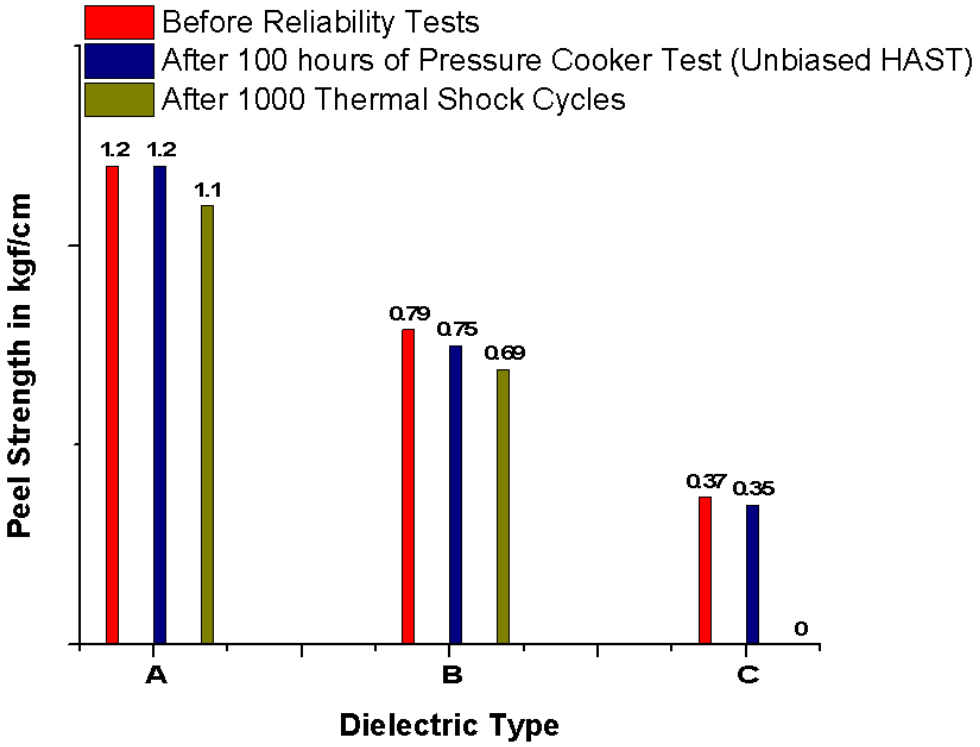


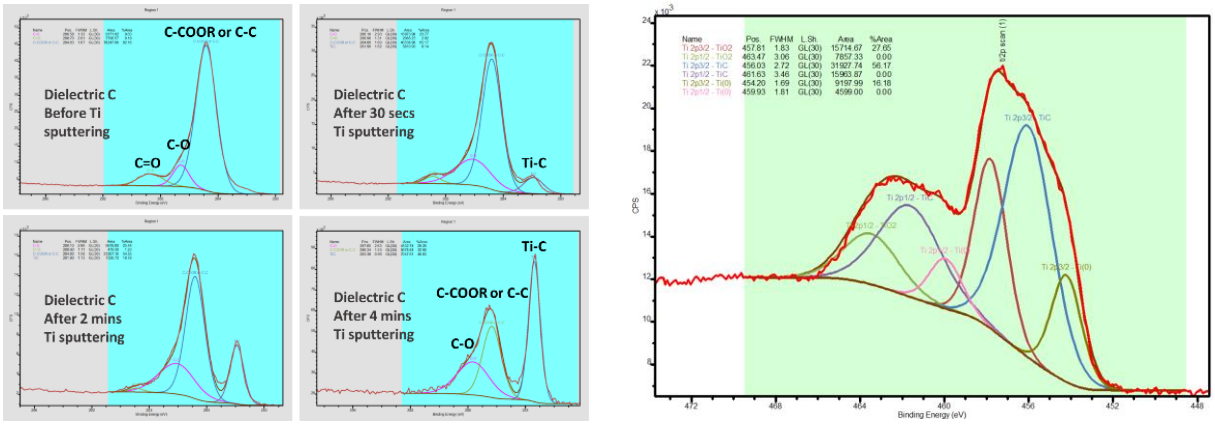
Figure 5-15: Peel strength values of sputtered titanium-copper seed to different dielectrics

As shown in Figure 5-15, the peel strengths range from 3.7 N/cm for dielectric C to 12 N/cm for dielectric A. To understand the variation in peel strengths, X-ray photoelectron spectroscopy (XPS) is used to characterize the interfacial bonds formed between Ti-Cu and polymer dielectrics. Fourier Transform Infrared Spectroscopy (FTIR) studies were done in Attenuated Total Reflection (ATR) mode for polymer dielectrics to characterize the presence of functional groups in these dielectrics. Based on these studies, the functional groups responsible for excellent Ti-Cu bonding would be established.

Figure 5-16 shows the formation of TiC peaks in the carbon C-1s region and TiC and TiO_x peaks in Ti-2p region. The atomic % of these compounds formed were not so different for all the three dielectrics. Further, FTIR spectra were collected for all the three dielectrics under ATR mode and the results are summarized in Figure 5-17. The higher percentage of phenoxy groups in

dielectrics A and B resulted in higher peel strengths than dielectric C. To validate this mechanism, a new dielectric D was formulated by modifying dielectric C and the peel strength of dielectric D increased to 1.1 kgf/cm (11 N/cm). The FTIR spectra of dielectrics C and D shown in

Figure 5-18 confirm the presence of phenoxy groups. Thus, TiC bonds formed with aromatic carbon in phenoxy group are resonance stabilized and lead to higher bond strength compared to TiC bonds formed with aliphatic carbon in acrylic resin. This study is useful for increasing the peel strength of copper to low-k non-polar polymer dielectrics for high aspect ratio RDL.



(A) **(B)**

Figure 5-16: XPS studies show (A) C-1s peaks confirming TiC bonds being formed with polymer dielectrics (B) Ti-2p peaks confirming TiO_x bonds being formed in addition to TiC bonds

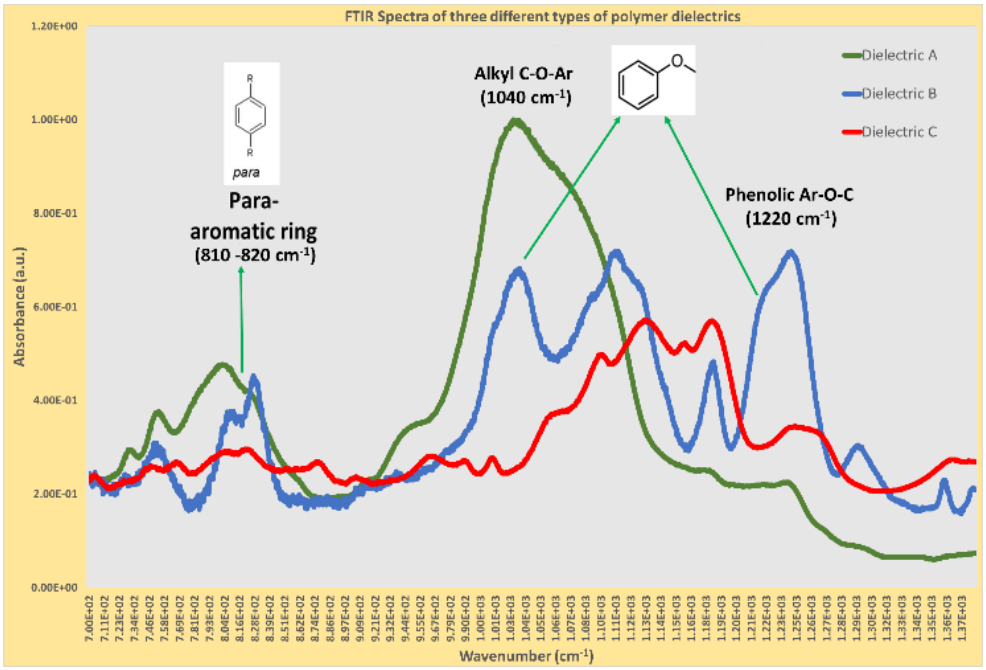


Figure 5-17: FTIR spectra of three different dielectric films

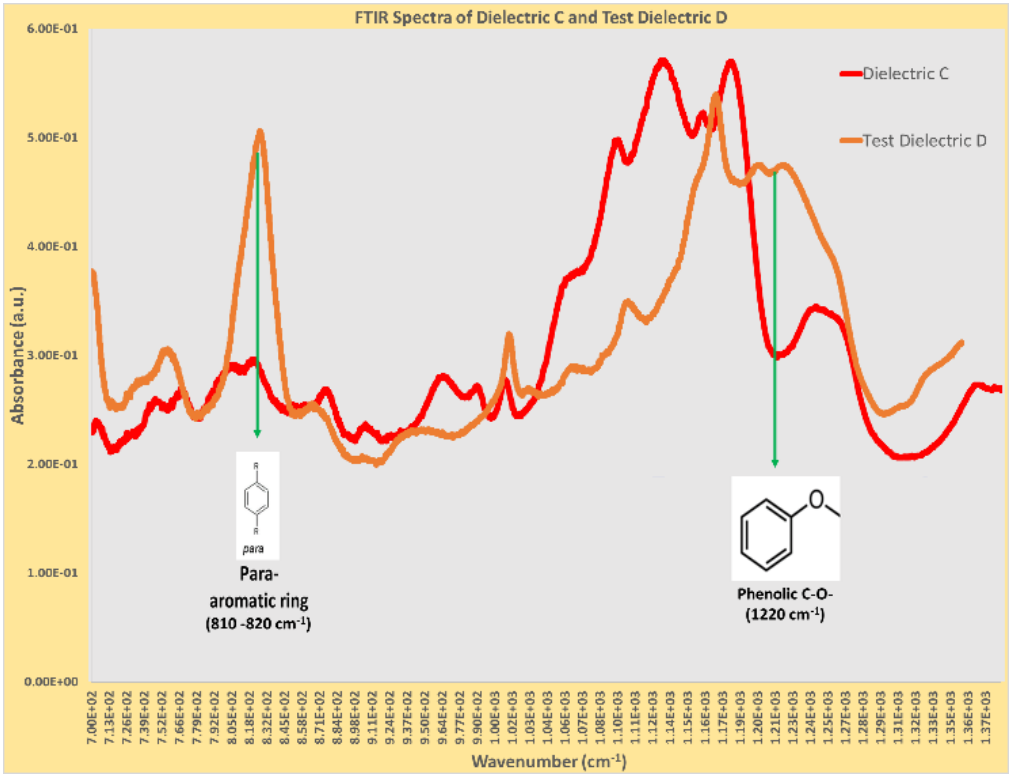


Figure 5-18: FTIR spectra of dielectrics C and D

5.3 Chapter 5 Summary

This chapter summarizes the properties of materials required for 2 µm multi-layer polymer RDL. The novel chemically amplified, positive-tone dry film photoresist materials were introduced for high aspect ratio 2 µm lithography. The material design for polymer dielectric materials was classified into two parts:

(A) Polymer dielectric material for fabrication of reliable 2 µm diameter microvias

The material design included modeling for varying CTE, modulus, tensile strength and % elongation to break properties of polymer dielectric for reliability of stacked three-layer microvias of 2 µm diameter. Based on the modeling results to prevent cracking in polymer dielectric or copper microvia, a novel photosensitive epoxy dielectric material with nano-silica filler (wt. % < 40) was developed with room temperature CTE of 35 ppm/K and modulus of 4 GPa. The maximum elongation that could be achieved was 6 % at 25 ^{0}C and the water absorption was 0.8 wt. %. The material has a combination of properties of CTE of high cure temperature polyimide and the modulus of epoxy with 38 wt.% silica filler. The tensile strength is similar to the epoxy with 38 wt.% silica filler of 95 MPa at 25 ^{0}C and 130 MPa at -55 ^{0}C. The % elongation to break is slightly higher than the epoxy equivalent. The low cure temperature for epoxy of 180 ^{0}C for 1 hour makes it an attractive candidate for low temperature processing. With these properties, it is necessary to have a tighter process control of maintaining taper angles between 70-90^0 during microvia fabrication.

(B) Polymer functional group with the ideal functional group for superior interfacial adhesion of sputtered titanium seed to polymer dielectric

The material design included modeling to identify the required peel strength for varying aspect ratio of 2 µm RDL with low CTE and high CTE dielectrics. The high CTE photosensitive

dielectrics primarily used for photo-embedded trench RDL usually have via-in-line structures with 2 μm RDL at an aspect ratio of 2.5-5. For such high aspect ratios, the required peel strength can be in the range of 0.5-0.7 kgf/cm. With this requirement, using acrylic and epoxy functional groups-based polymer dielectrics, the mechanism of titanium seed bonding with polymer dielectric was established using XPS studies. TiC and TiO_x bonds were formed at the metal-polymer interface and the strength of the bonds determine the peel strength and the reliability of these bonds to thermal cycles. FTIR studies predicted the presence of phenoxy groups in high peel strength polymer dielectrics. The dielectric C with low peel strength was modified to dielectric D by the addition of phenoxy group and the peel strength of dielectric D increased to 1.1 kgf/cm. The proposed mechanism was validated and a design pathway for superior interfacial adhesion of titanium sputtered seed with low-k dielectrics was established.

CHAPTER 6. PROCESSES FOR 2 µm MULTI-LAYER POLYMER RDL

This chapter will describe the most advanced processes for fabrication of 2 µm multi-layer polymer RDL.

6.1 Semi-Additive Process (SAP) versus embedded trench RDL

The process flow for SAP was shown in Figure 1-8 (A). In section 2.4 (Figure 2-15), the side-etch due to SAP RDL with novel seed layer etch chemistries was quantified [[39], [40]]. A layer of 50 nm thick titanium barrier layer and 200 nm thick copper seed layer was sputtered on a smooth polymer dielectric (R_a < 40 nm and R_z < 100 nm) laminated on a glass panel. The challenge of high aspect ratio RDL with SAP is mainly attributed to the seed layer etch process. The side-etch profiles of 2 µm width, high aspect ratio copper lines after seed layer removal using a novel differential copper seed etchant are characterized using cross-sectional SEM. Figure 6-1 shows the minimal side-etch (tapered profile) with no over-etch and residues between 2 µm copper lines with aspect ratio of 3. The lines were subjected to further seed layer etch process to remove the copper residues. The tapered side-etch worsens with 100 % over-etch as shown in Figure 6-2.

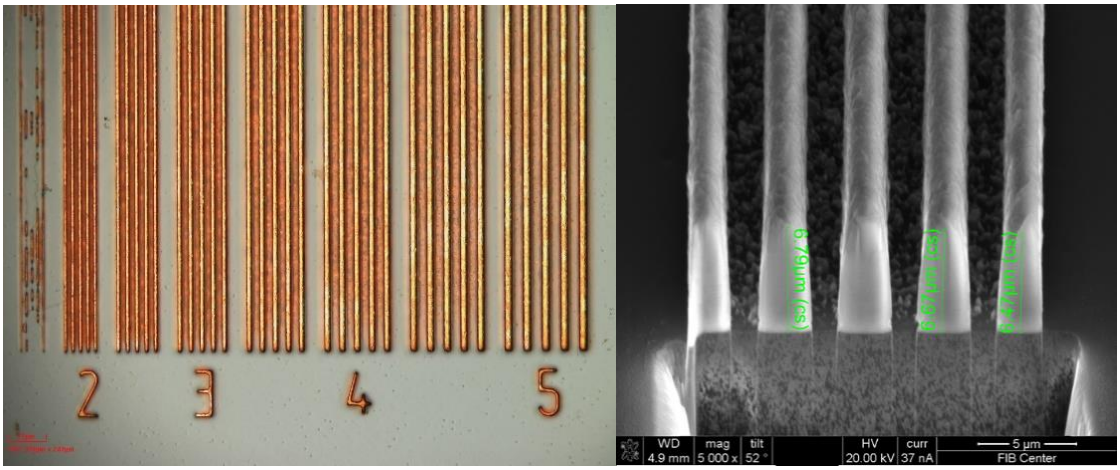


Figure 6-1: Seed layer residues between high aspect ratio 2 µm width copper lines with tapered profile due to seed etch with no over-etch (higher resistance for tapered lines)

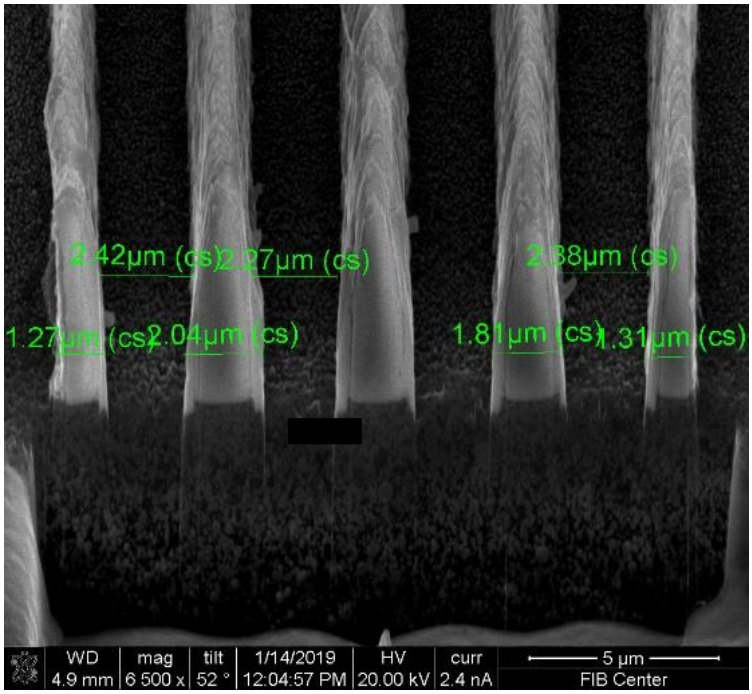


Figure 6-2: Tapered profile of copper lines due to seed etch with 100 % over-etch (higher resistance for tapered lines)

Embedded trench RDL is demonstrated as an alternative to SAP RDL to provide zero side-etch. A process flow of embedded trench RDL using a photosensitive dielectric is shown in Figure 6-3. This type of RDL is similar to the BEOL damascene process but with organic polymer dielectric. The planarization process is a mechanical fly-cut process using Disco Surface Planar tool instead of the chemical mechanical polishing (CMP) process for silicon BEOL RDL. Embedded trench process with chemically amplified photosensitive dielectric for 2 µm RDL with an aspect ratio of 2 was demonstrated as is shown in Figure 6-4. A multi-layer with via-in-trench structure using organic damascene RDL process flow is shown in Figure 6-5, where the aspect ratio of microvia and trench layer is two each. Hence, there is the necessity of high peel strength discussed in Table 5-11 for such high aspect ratio RDL structures. A cross-section of the embedded trench RDL with aspect ratio of 1 using excimer laser process is shown in Figure 6-6. The

advantage of such a process is that excimer laser can be used to pattern even in low CTE non-photosensitive polymer dielectrics requiring lower peel strength values to prevent interfacial delamination.

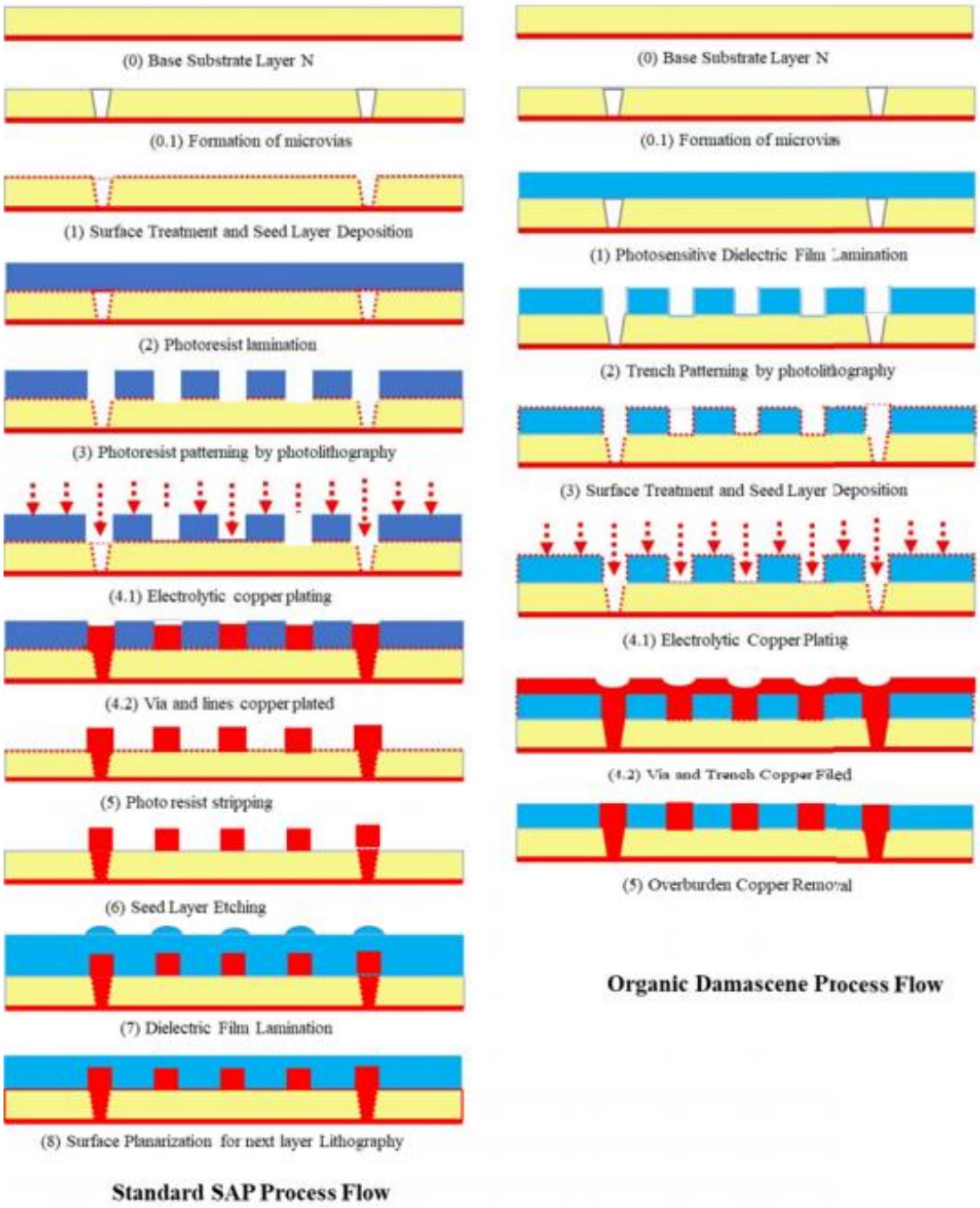


Figure 6-3: Process Flow for Standard SAP versus Organic Damascene RDL [60]

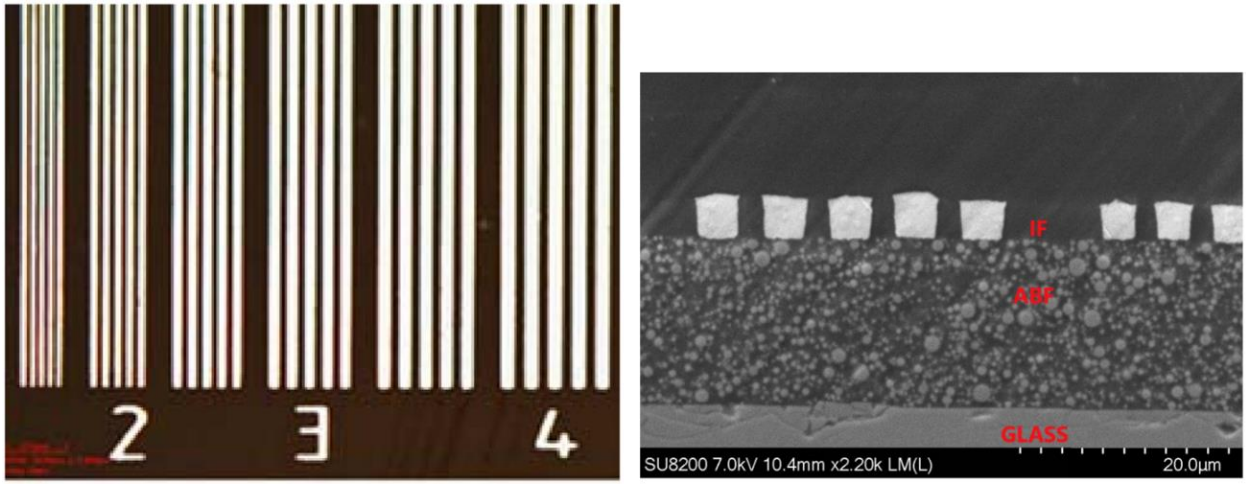


Figure 6-4: Embedded trench process with dry film photosensitive dielectric for 2 µm RDL with aspect ratio of 2 (IF refers to insulating film photosensitive dielectric and ABF refers to Ajinomoto Build-Up film)

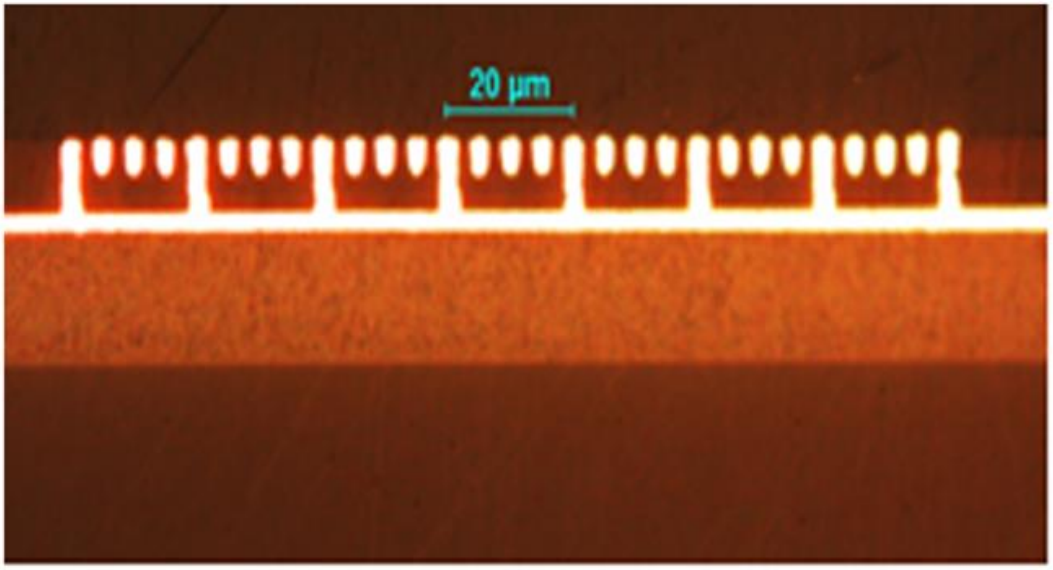


Figure 6-5: Via-in-trench structure using organic damascene RDL process flow for 2 µm line width, 2 µm space and 2 µm microvias. The via-in-trench 2 µm RDL structure has a total aspect ratio of 4.

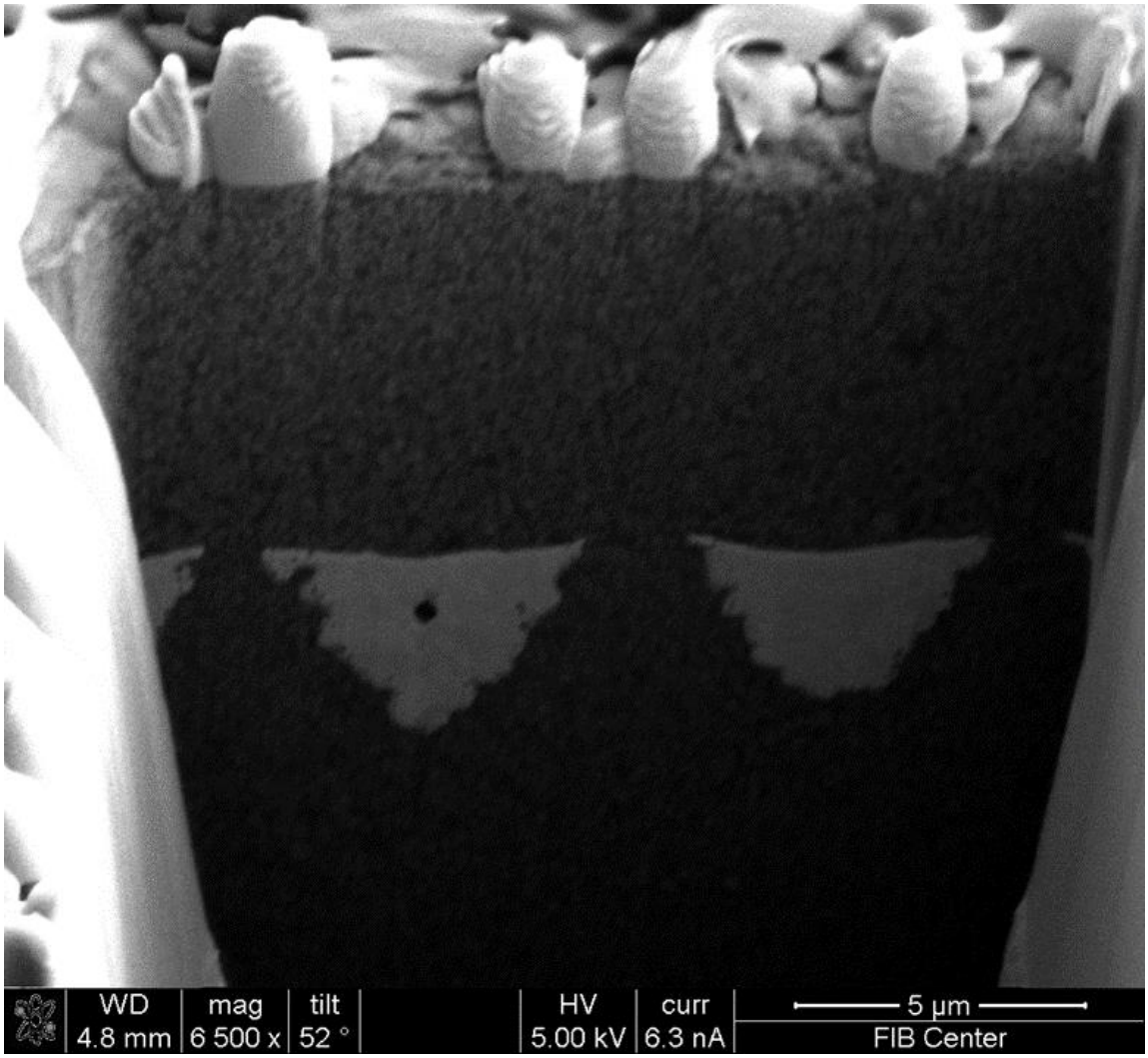


Figure 6-6: Embedded trench RDL with 4 µm line width and 2 µm space at an aspect ratio of 1 using excimer laser process in non-photosensitive dielectrics

The limitation of embedded trench RDL process seem to be scaling down below 2 µm RDL due to the resolution of photosensitive dielectric or excimer laser patterning. Excimer laser-based trenches could also be scaled down to 2-2.5 µm width trenches using no filler-based dielectrics with an aspect ratio of 1. The embedded trench RDL process with sputtered seed is not easy to scale owing to lots of delaminations as a result of the high peel strength required to maintain such high aspect ratio, fine pitch RDL structures during the planarization process. Also, the presence of hard titanium barrier seed makes it difficult for the Surface Planar tool since it is not designed to

shear through hard metals. Embedded trench structures with electroless copper seed layer (no titanium barrier as shown in Figure 6-6) were reliably planarized using a low CTE polymer dielectric (non-photosensitive) over an entire 300 mm wafer with 98 % yield. However, the minimum resolution of the trench achieved was 4 µm width due to the desmear etch step which is used to roughen polymer dielectrics during the electroless copper seed deposition process.

To summarize, the type of dielectric determines the minimum resolution that can be patterned in organic damascene RDL process flow. With non-photosensitive dielectrics, excimer laser is used to pattern 2-4 µm width trenches while with photosensitive dielectrics, UV photolithography (365 nm) is used to pattern 2 µm width trench RDL. The embedded trench RDL suffer from the following limitations: (1) The resolution is limited to 2 µm in 5 µm thick dielectrics and there is a very limited amount of such dielectrics available. This is because dielectrics are permanent structures in the final RDL and hence, have been designed for ideal mechanical, chemical, thermal and electrical properties. The tight control of properties is not required for photoresist materials since they are temporary and stripped away once the patterning process is complete. This allows photoresist materials to be designed carefully for the best resolution that can be achieved. Hence, high aspect ratios (> 2) with embedded trench RDL is not possible, (2) The planarization process requires the blade to cut through a titanium barrier layer while the Surface Planar planarization tool is designed for soft and ductile materials like polymer and copper. Also, as discussed in Table 5-11, the requirements for peel strength with high aspect ratio, 2 µm RDL with high CTE photosensitive polymer dielectrics present significant challenges for interfacial adhesion. Thus, there are delamination failures with sputtered Ti-Cu seed in embedded trench RDL during the planarization process. This is shown in Figure 6-7.

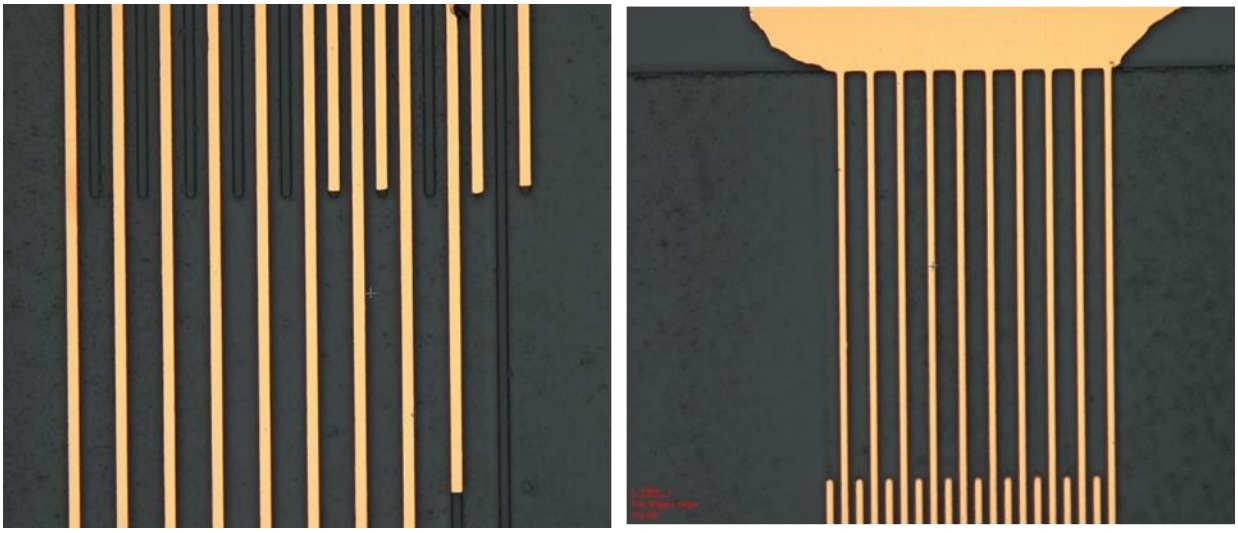


Figure 6-7: Delaminations due to planarization process in embedded trench RDL with sputtered Ti-Cu seed layer

6.2 Novel sidewall protected RDL for zero-side etch process during seed layer removal

Considering the above challenges, the proposed research demonstrates a novel seed etch process to fabricate high aspect ratio copper traces with polymer SAP RDL. The proposed novel process flow is shown in Figure 6-8. The parylene dielectric with low dielectric constant (D_k ~ 2.2-2.6) will lower the capacitance between the traces. In this study, parylene-N was used to show the proof of concept due to its easy availability (D_k ~ 2.65, D_f < 0.005). Ideally, parylene-F with better electrical properties (D_k ~ 2.3, D_f ~ 0.003) can be used as well for this structure.

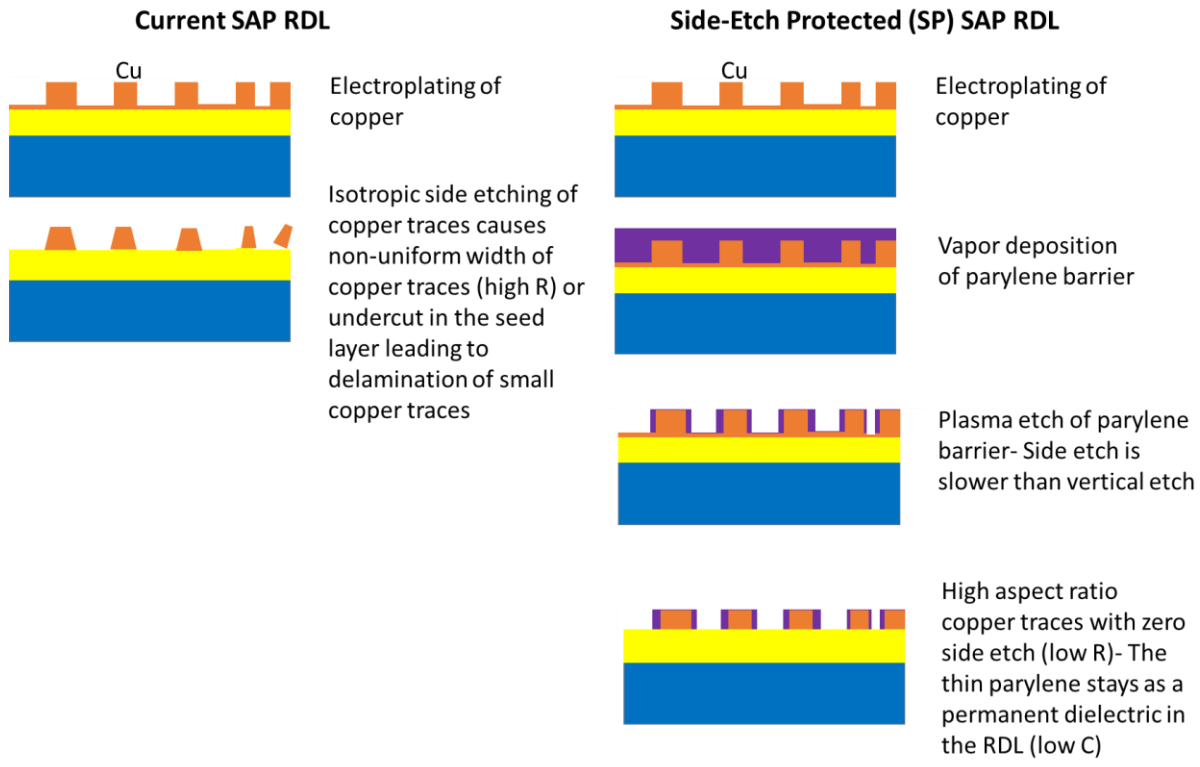


Figure 6-8: Proposed process flow for zero side-etch copper lines

The zero-side etch process was therefore developed to overcome the challenge of fabricating high aspect ratio copper lines without any taper to maintain signal quality using SAP RDL processing. As seen in section 5.1, there are novel photoresist materials to ensure high aspect ratio lithography for RDL down to 1 µm line width and 1 µm space. However, seed layer removal from such fine space structures with aspect ratios of 4-5 is challenging without affecting the cross-sectional profiles of copper lines. Figure 6-9 shows the cross-sectional view of copper lines after seed layer etch process with the novel side-etch process. As shown in Figure 6-9, the sidewalls of the copper lines are protected by the parylene layer and hence, there is no side-etch of the copper traces. The 5 µm line width and space profile was seed layer etched three times (200 % over-etch) to ensure that there is no side-etch and no delamination of parylene layer from the sidewalls. This

also ensures that there are no residues of copper seed remaining in high aspect ratio, fine pitch RDL structures.

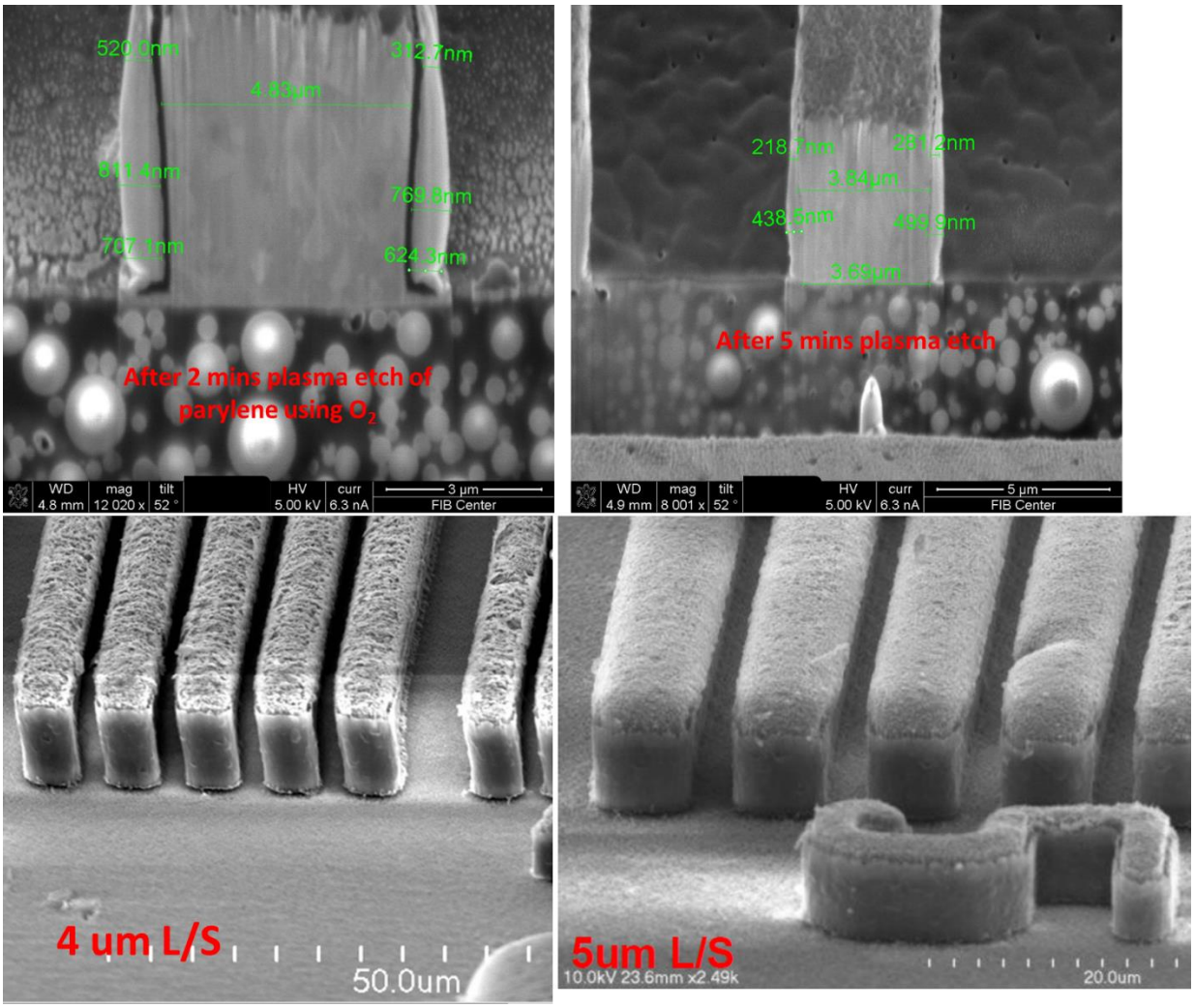


Figure 6-9: Zero side-etch seed removal process with sidewall protected SAP RDL. The sidewalls highlight the thin 200-300 nm parylene layer (after 5 mins O_2 plasma etch) to protect the copper line during seed layer etch process.

6.3 Novel process to scale microvia diameters to sub 1-micron

With regards to scaling down of microvia diameters, the proposed research demonstrates 2-5 µm diameter microvias using laser and photolithography processes. The via patterning using a high CTE photosensitive polymer dielectric down to 2 µm diameter photovia was shown in

Figure 6-5. A similar structure can be patterned using excimer laser process, which is shown in Figure 6-10. With the nano-silica filled, low CTE photosensitive epoxy-based polymer dielectric developed as an ideal candidate material in section 5.2.1, the microvias formed are in the range of 2-3 µm diameters with varying taper angles from 55^0-80^0. However, as discussed in section 5.2.1, the taper angles need to be above 70^0 for excellent polymer and copper reliability with such a dielectric. Thus, it is necessary to tune tightly the microvia fabrication process window.

As discussed above, the scaling down of minimum resolution that can be patterned in the dielectric is not easy and hence, the minimum microvia diameters that have been demonstrated in production are in the range of 6-10 µm [[6], [7], [32]. This research proposes a novel process flow which goes on as an extension with the proposed process flow in Figure 6-8. This process uses photoresist materials discussed in section 5.1 to enable formation of sub 1-micron diameter microvias with 85^0-90^0 taper angles. The novel process flow to build sub 1-micron multi-layer RDL using SAP in polymer dielectrics is shown in Figure 6-12. This breakthrough in RDL process will enable scaling of SAP RDL to high aspect ratio, sub 1-micron width copper lines and microvias. The polymer dielectric in this process is only used for filling the gaps as an insulator and hence, can be designed as a material with ideal electrical, mechanical, thermal, chemical properties and with excellent adhesion to copper.

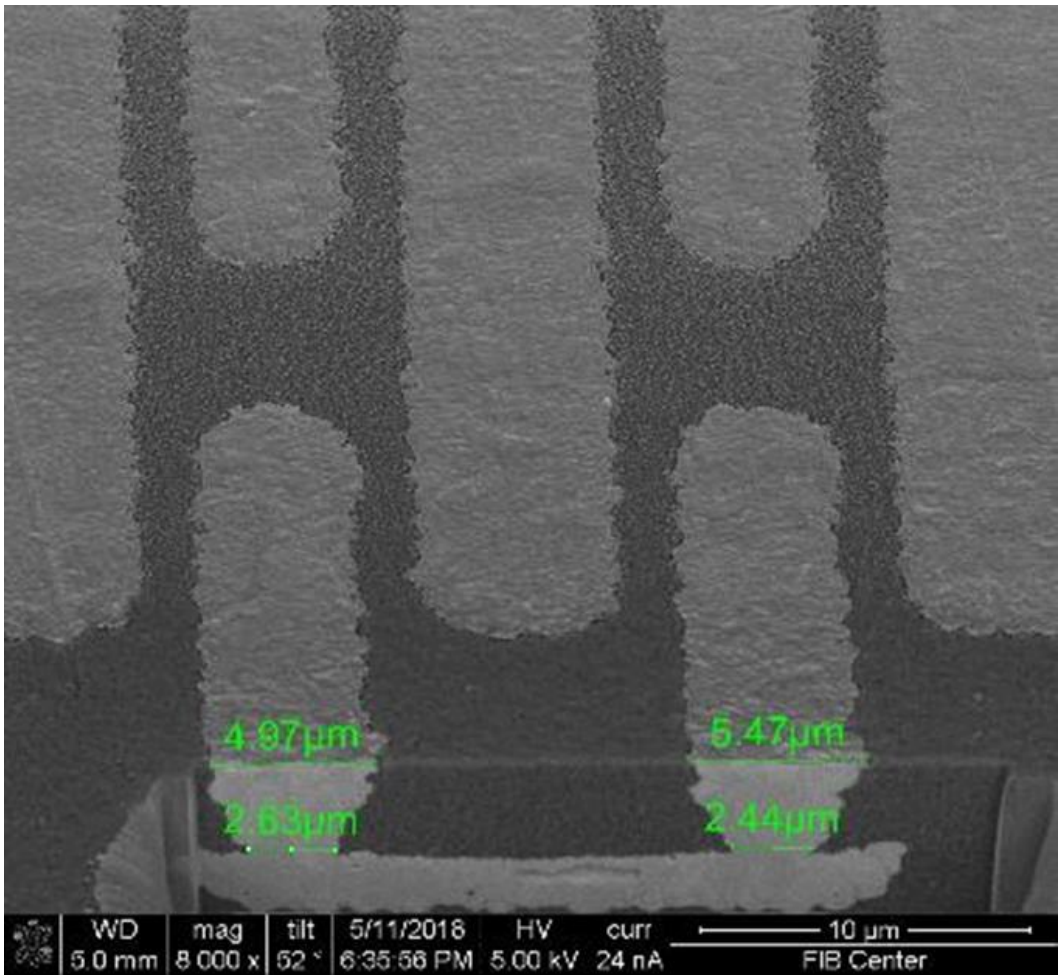


Figure 6-10: Excimer laser via-in-trench structure showing 3 µm bottom via diameter in low CTE non-photosensitive polymer dielectric

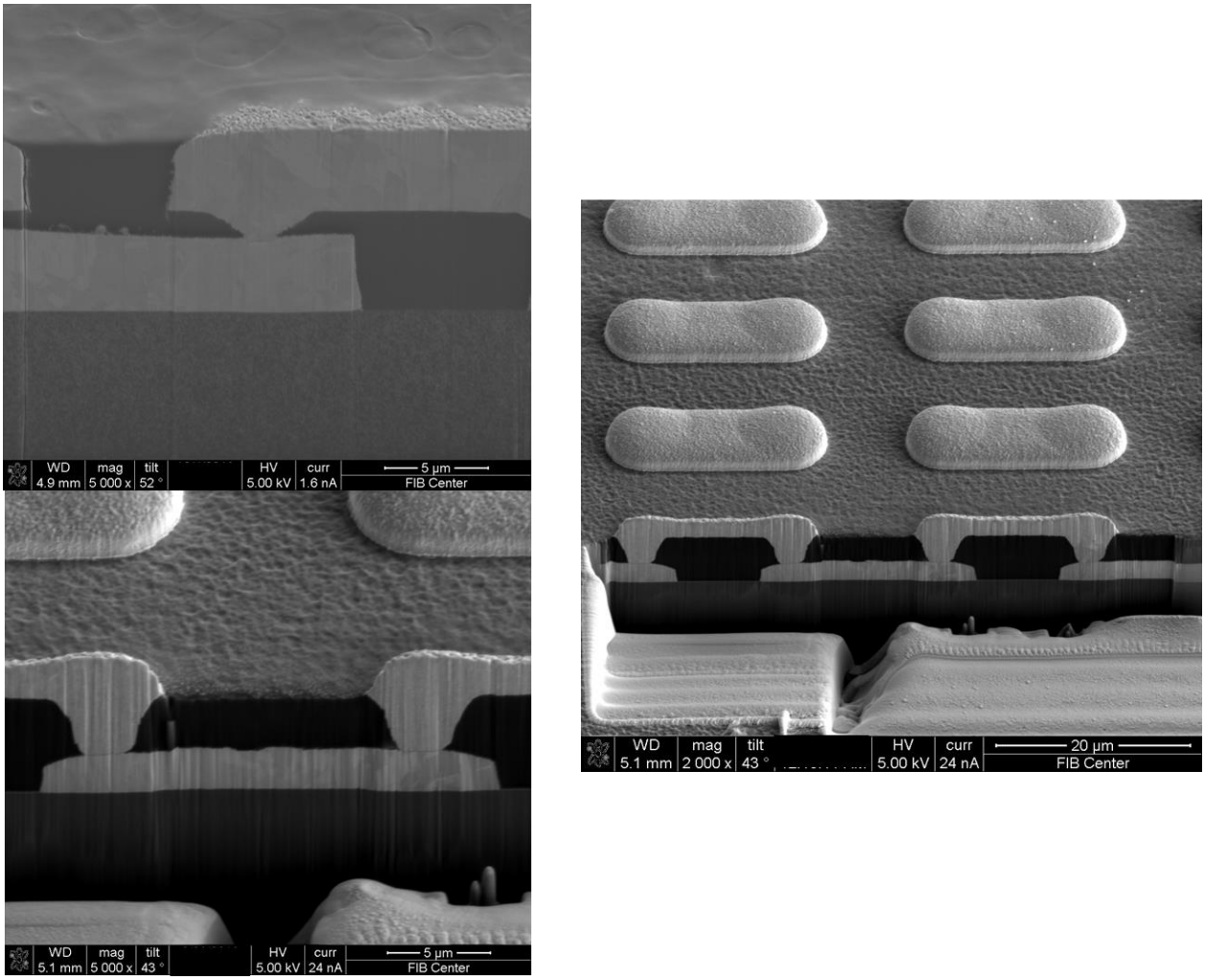


Figure 6-11: Photolithographic patterning of 2-3 µm diameter photovias with various taper angles (55^0-80^0) in the low CTE nano-silica filled epoxy photosensitive dielectric

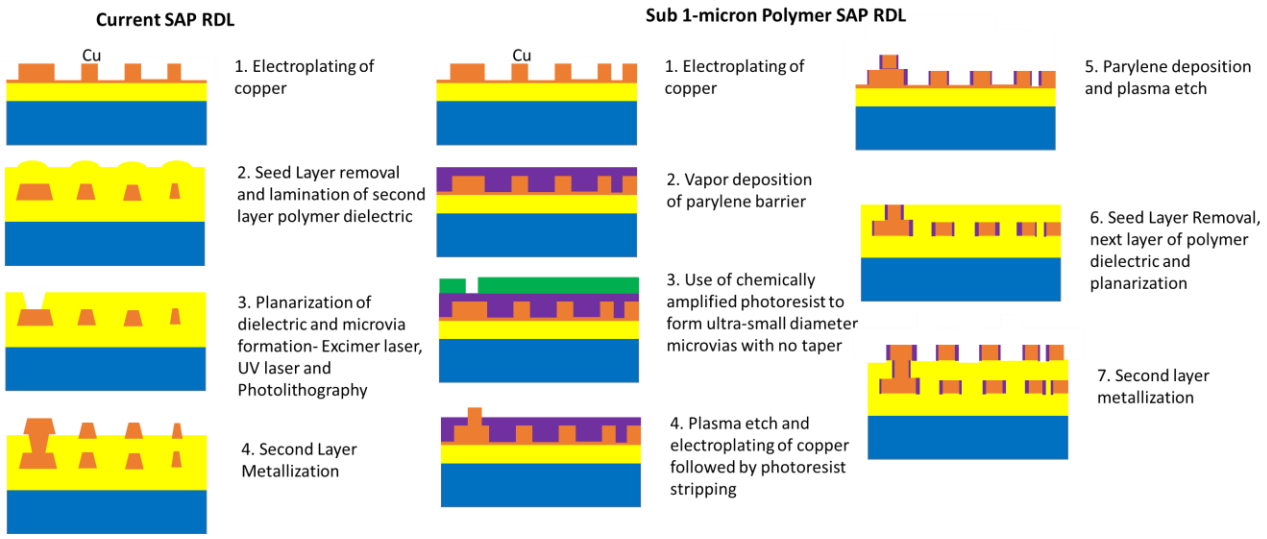


Figure 6-12: Proposed novel process flow for sub 1-micron SAP RDL

The structure after vapor deposition of parylene dielectric (step (2) of the novel process flow in Figure 6-12) is shown in Figure 6-13. This shows complete filling of the fine spaces after parylene vapor deposition. The thickness of parylene above the copper lines is ~ 2 µm. The thickness of the copper lines is ~ 5 µm. Due to the non-availability of a separate via mask, the same mask was used again to pattern on top of the first metal layer RDL structures. The small misalignment of the projection stepper tool (+/- 1-2 µm) during step (3) of the process flow shown in Figure 6-12, resulted in parylene being plasma-etched from the undesired space areas as indicated in step (4). The structure after electroplating (step (4)) shown in Figure 6-14 validated the success of this novel process. The via was plated to a thickness of 7 µm to test the process for any delaminations. In real structures, the typical via thickness would be only 1-2 µm and can be controlled very easily for fully-filled vias using this process. The plating in unwanted areas in Figure 6-14 were due to zero alignment tolerance and can be removed by using a capture pad of 5 µm for 2 µm microvia structure.

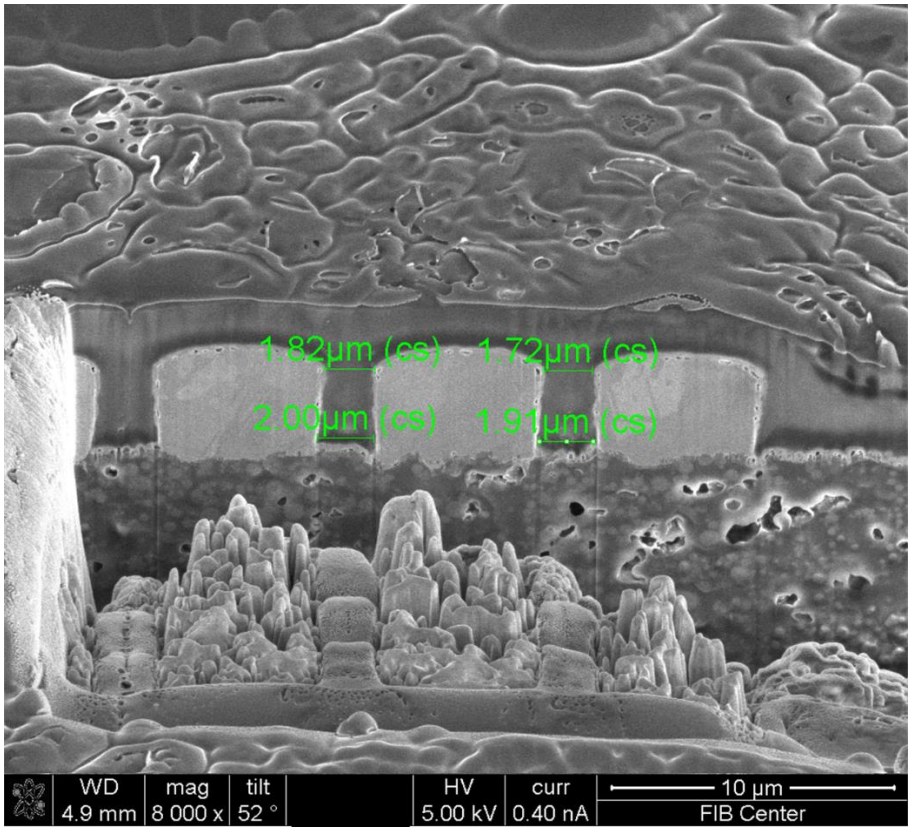
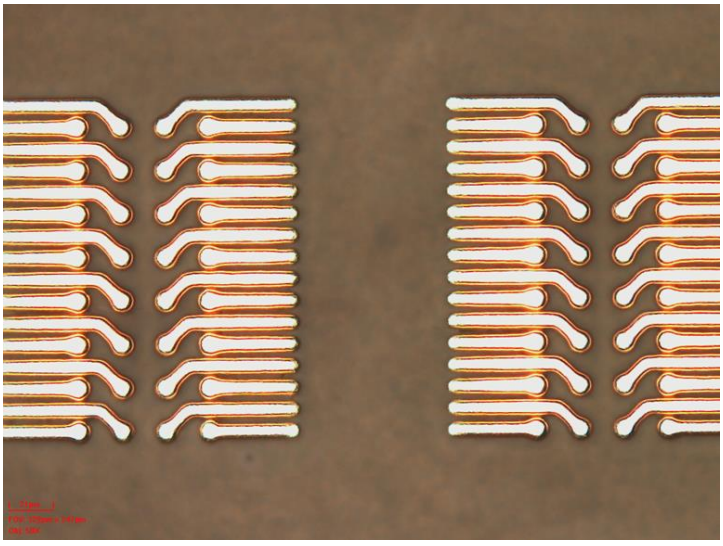
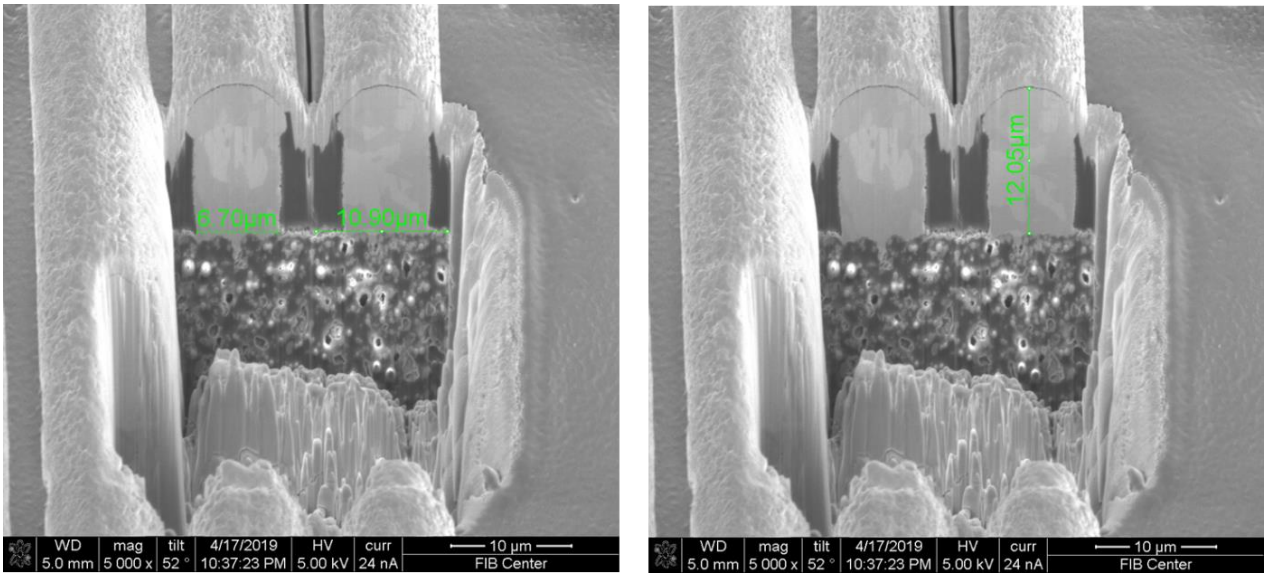


Figure 6-13: Fine pitch polymer RDL after vapor deposition of parylene. The wrinkles on the surface are due to the melting of polymer from heat during focused ion beam (FIB) processing.



(A)



(B)

Figure 6-14: Structure of direct via plating on the line (After step (4) of the process flow shown in Figure 6-12) (A) With excellent alignment 3 µm line and space structure stacked on top of each other and (B) With +/-2 µm alignment shifts showing removal of parylene from undesired areas during plasma etch leading to plating in these areas (can be avoided with 5 µm capture pads for 2 µm vias)

6.4 Chapter 6 summary

This chapter discussed about semi-additive process and its challenges in seed layer etch process to scale to 2 µm RDL. Embedded trench RDL using photosensitive dielectric and excimer laser based embedded trench RDL using non-photosensitive dielectric was evaluated. The challenges in planarization for embedded trench RDL were identified and the need for a novel zero-side etch process to scale SAP RDL was identified. A novel process using a parylene barrier was demonstrated with zero side-etch to scale SAP RDL even to sub 1-micron RDL. Microvia processes to scale diameters below 5 µm with vertical taper angles (close to 90^0) were found to have a very tight process window. Also, the limitation of a minimum 2 µm bottom diameter of microvia was observed for both photosensitive dielectrics and excimer laser drilled non-

photosensitive dielectrics. Thus, a novel process flow was demonstrated to scale microvia diameters to even sub 1-micron dimensions using photoresist patterning instead of dielectric patterning.

CHAPTER 7. RELIABILITY OF 2 µm MULTI-LAYER POLYMER RDL

The reliability of 2 µm RDL comprises of two main components: (A) Electrical reliability of polymer RDL with 2 µm line width and 2 µm space and, (B) Thermal cycling reliability of 2 µm diameter microvias.

7.1 Electrical reliability of copper lines at 2 µm space with polymer RDL

Copper lines are fabricated in a meander pattern with comb structures using excimer laser trench RDL process described in chapter 6. The comb structures in the fine pitch RDL had an area of 0.4 mm x 0.4 mm. The leakage current between the lines are measured under a glove box environment with H_2O content of less than 0.5 ppm and O_2 content below 50 ppm. The structures involve RDL copper lines fabricated using the same polymer dielectric with both electroless copper seed and Ti-Cu seed layers. The effect on leakage currents due to different polymer dielectrics with varying moisture absorption values is also evaluated with sputtered Ti-Cu seed layers. The samples with RDL copper line structures are subjected to first pre-conditioning as per JEDEC JESD 22- A113 which involves baking at 125 ^{0}C for 24 hours followed by moisture soak (Level 3: 60 ^{0}C, 60% RH for 40 hours) and finally three cycles of lead-free solder reflow with a peak temperature of 260 ^{0}C. The samples are then exposed to biased highly accelerated stress test (bHAST) conditions (130 ^{0}C, 3.5/ 5 Volts, 100 hrs) as per JEDEC JESD 22- A110 and the leakage currents are measured again to test for electrochemical migration of copper between the lines. Leakage currents of above 1 µA after bHAST conditions are considered to be failed. The cross-sectional schematic of the comb structure to be tested for electrochemical migration reliability using copper line and space RDL structure with polymer dielectrics is shown in Figure 7-1.

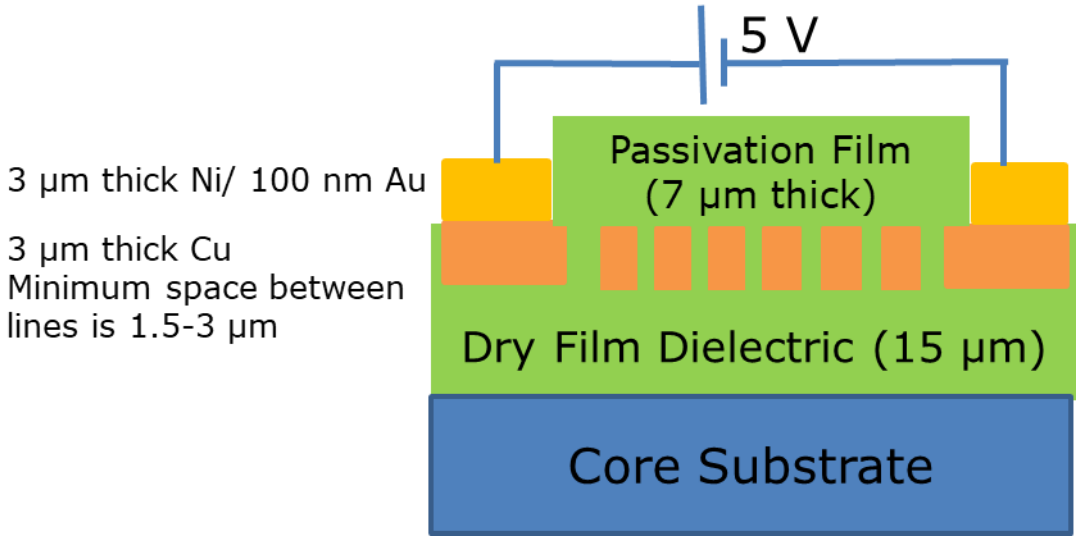


Figure 7-1: Test structure to study electrochemical migration reliability of copper lines and spaces with polymer RDL

Two dielectrics were used for the above test structure: (i) Polymer dielectric A with 0.6 wt. % moisture absorption using both electroless copper and Ti-Cu sputtered seed layers and, (ii) Polymer dielectric B with 1.5 wt.% moisture absorption with sputtered Ti-Cu seed layer. Both the dielectrics are designed for halogen content below 10 ppm to prevent any copper dendritic failures as discussed in section 2.5. The halogen content is measured in two ways: (A) Combustion method for the total halogen content (specifically chlorine) in the dielectric and, (B) Pressure cooker extraction method for water soluble halogen content (specifically chlorine). The total soluble content of halogens (especially chlorine) as measured from method (B) affect electrochemical migration reliability and are reported here as below 10 ppm in polymer dielectrics. The RDL design was classified into two: (i) 3 µm line width and 4 µm space and (ii) 4 µm line width and 6 µm space. However, due to RDL processing with excimer laser-based trenches, the fabricated structure for design (i) had a minimum spacing of 1.5 µm and the minimum spacing for design (ii) was 3 µm. The leakage current characteristics of the samples with polymer dielectrics A and B using sputtered titanium and copper seed and with polymer dielectric A using electroless copper seed

were studied after fabrication. These are shown in Figure 7-2, Figure 7-3 and Figure 7-4 respectively. While the leakage behavior of polymer dielectrics A and B with sputtered Ti-Cu seed layers were not much different after fabrication, the leakage behavior of polymer dielectric A with electroless copper seed layer at 1.5 µm space showed an electrical spark behavior during 0 to 40 V scans. The leakage current would shoot up momentarily and come back to normal 1 nA leakage current at smaller voltage levels. This behavior was predicted due to the rough edges present in the polymer dielectric due to wet permanganate desmear etch process used to roughen the polymer dielectric for reliable bonding of electroless copper seed to polymer dielectric. This concept is shown in Figure 7-5.

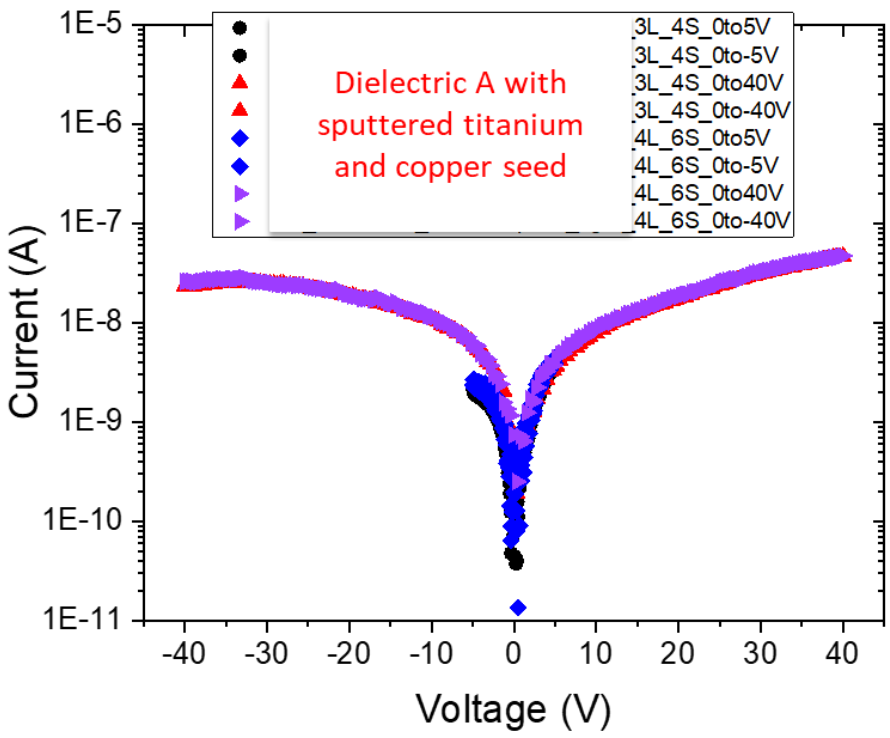


Figure 7-2: Leakage of RDL with polymer dielectric A using sputtered titanium and copper seed

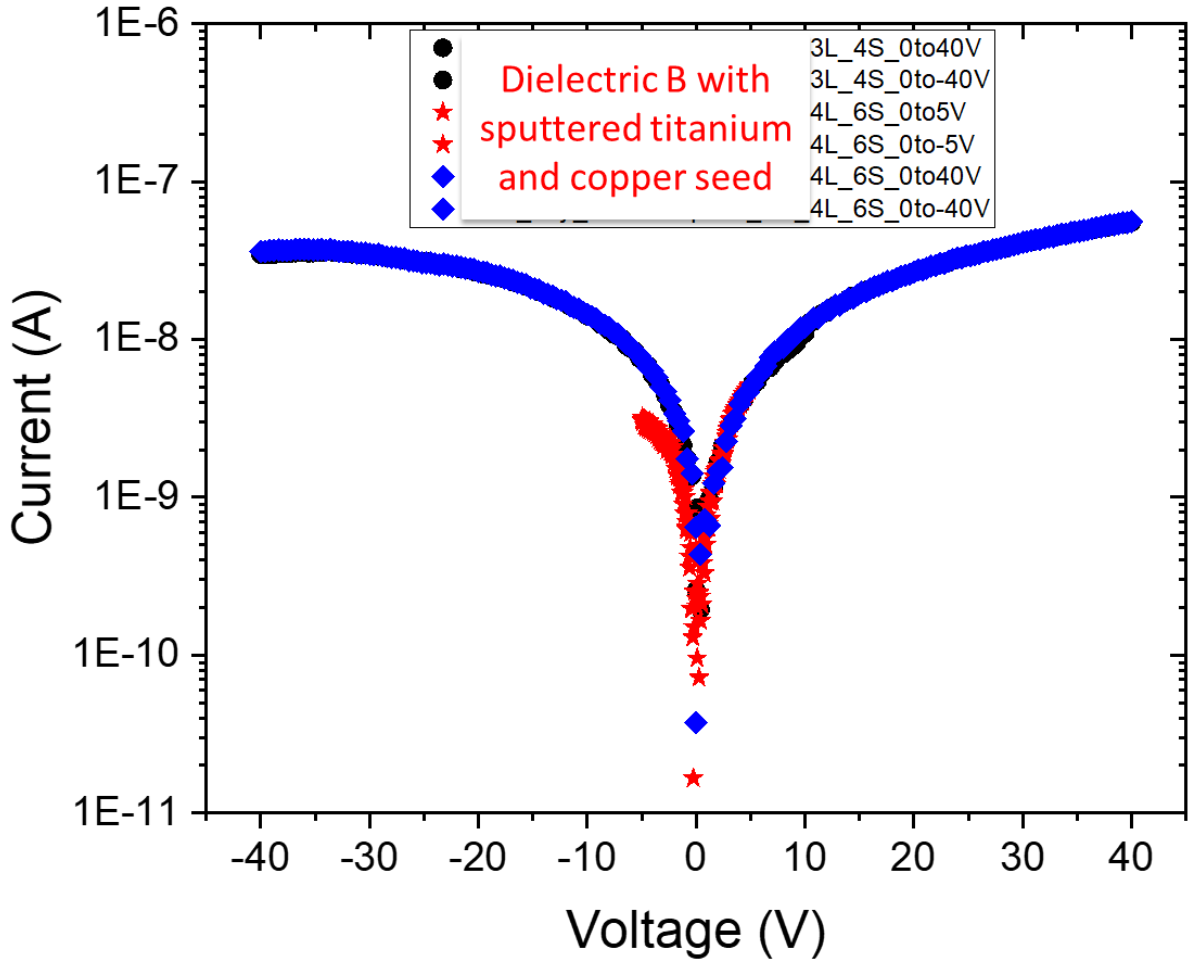
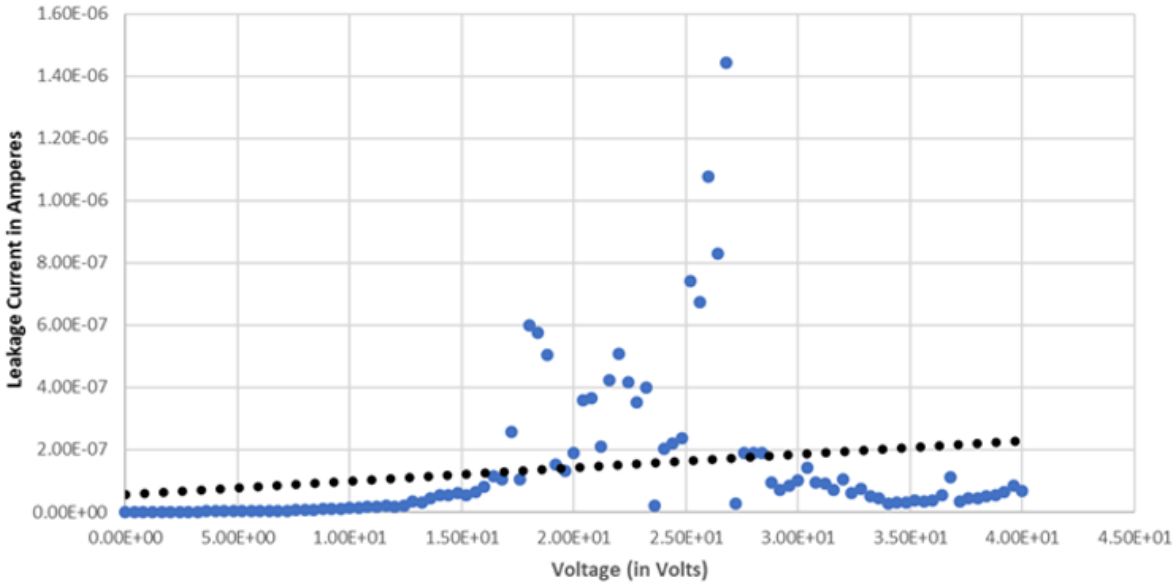
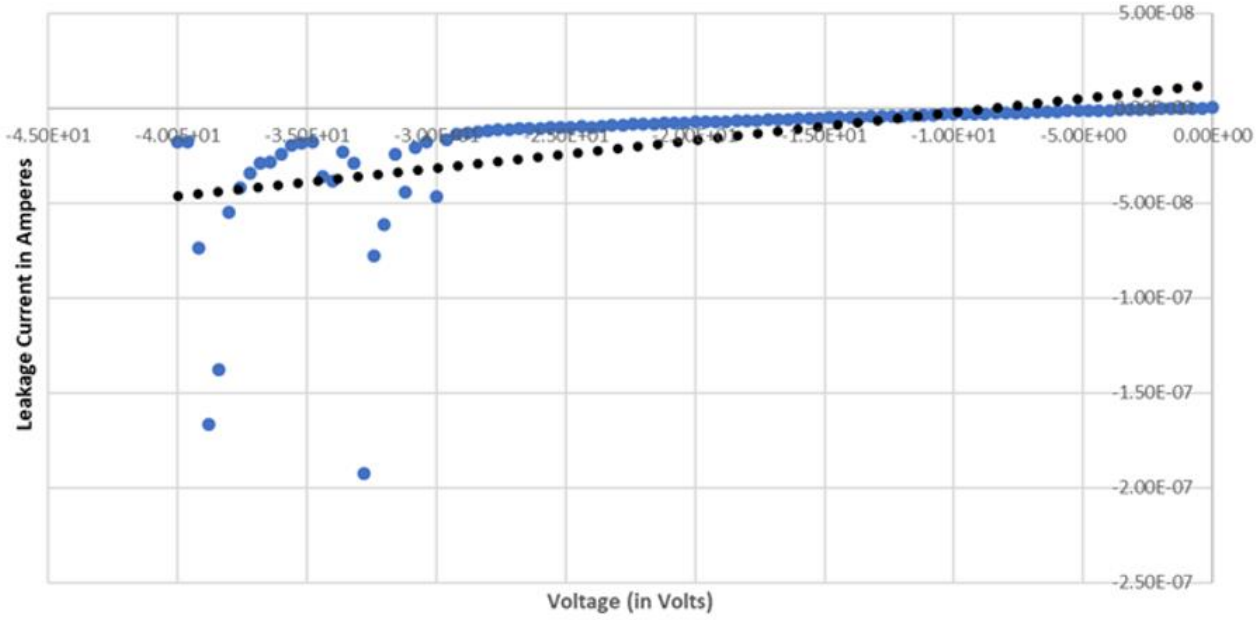


Figure 7-3: Leakage of RDL with polymer dielectric B using sputtered titanium and copper seed



(A)



(B)

Figure 7-4: Leakage behavior of RDL showing sparks with polymer dielectric A using electroless copper seed for 1.5 µm space RDL design (A) 0 to 40 V scan (B) 0 to -40 V scan

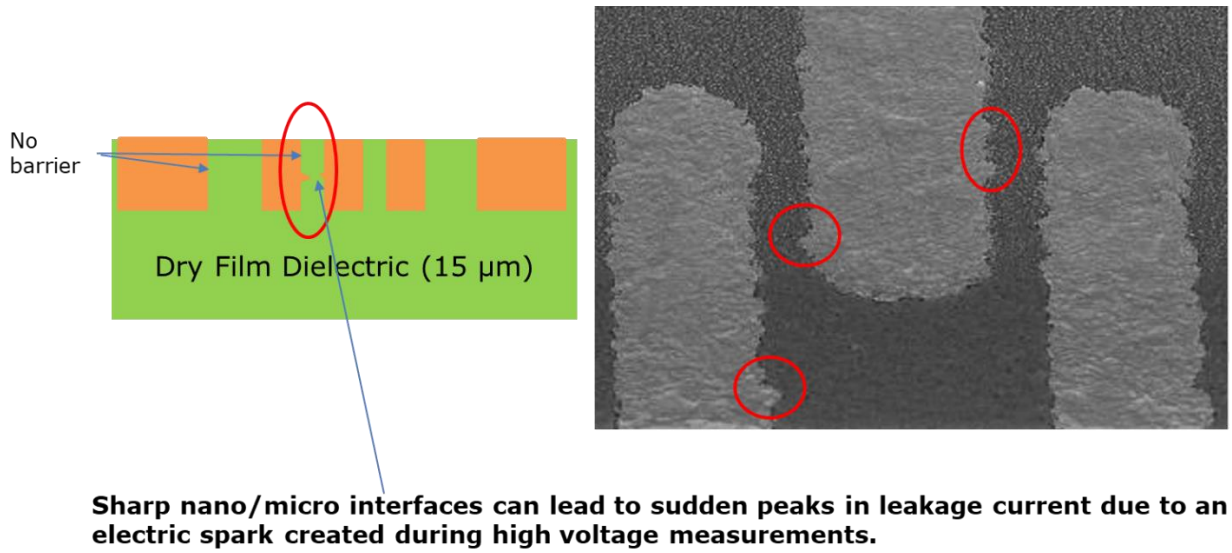
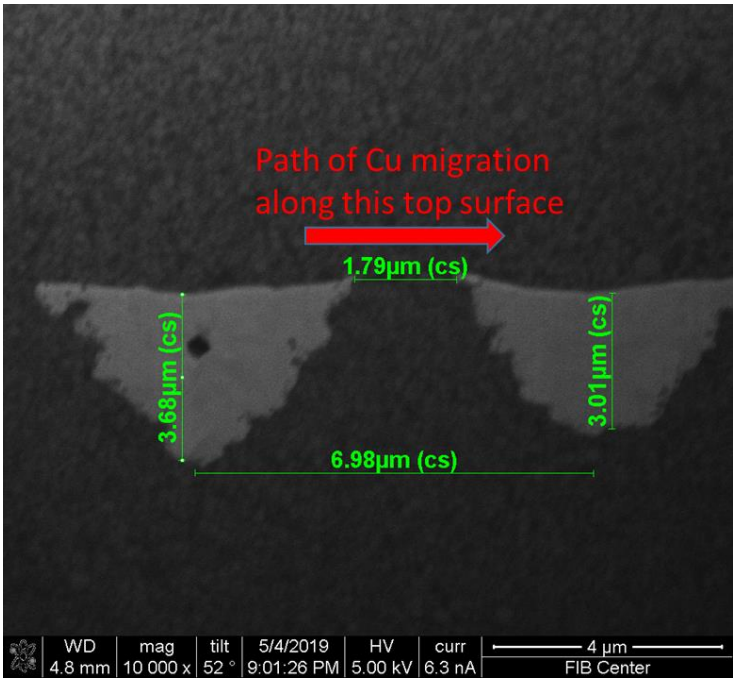
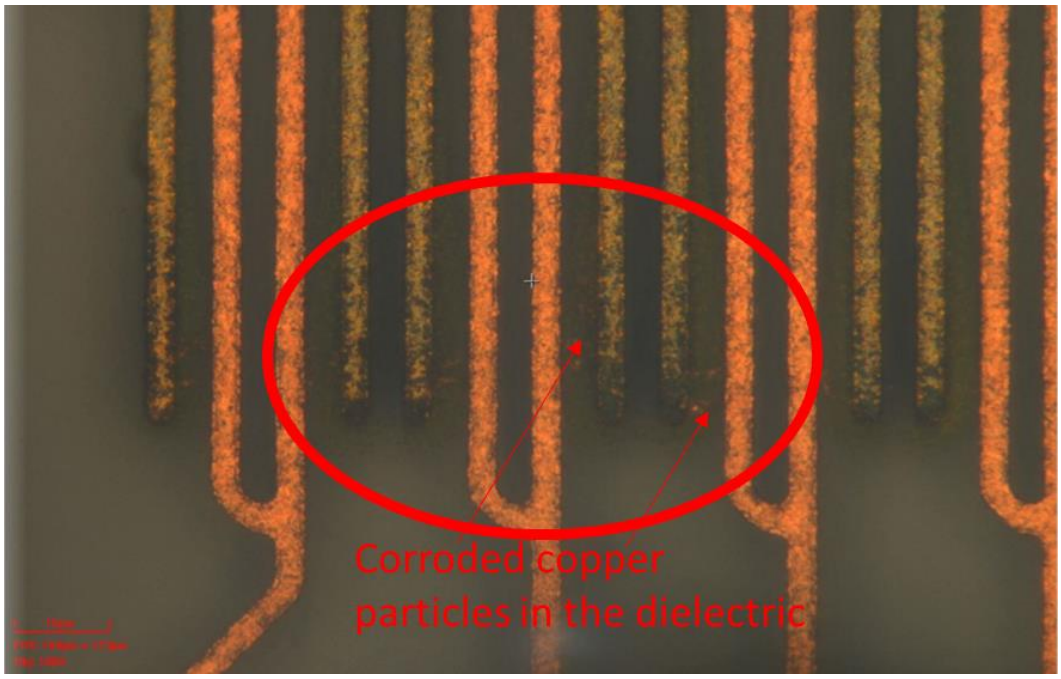


Figure 7-5: Possible cause for spark behavior in electroless copper RDL at 1.5 µm space during high voltage scans

The samples were subjected to biased HAST under 5 V after the preconditioning cycles. The result for design with 3 µm space with polymer dielectric A passed the criteria of leakage resistance of 1 MΩ after 150 hours of biased HAST at 5V. The result for design with 1.5 µm space with polymer dielectric A showed failure with a leakage resistance of 1 MΩ after 80 hours of biased HAST at 5V. Both the sputtered Ti-Cu seed and electroless copper seed layer samples failed around the same time. This is because the minimum space was on the topmost surface layer of the RDL and the copper oxide particles migrated along the top surface of polymer. The sample with dielectric B showed failure within 10 hours of biased HAST at 5V. The failure mechanism was similar with copper oxide particles migrating along the top surface of dielectric. This is shown below in Figure 7-6. The leakage current behavior of dielectric A after 100 hours of biased HAST could be only measured as shown in Figure 7-7 since dielectric B showed complete electrical short after 10 hours of biased HAST.



(A)



(B)

Figure 7-6: Electrochemical migration failure of copper at 1.5 µm space with polymer dielectric A in 80 hours of biased HAST at 5V

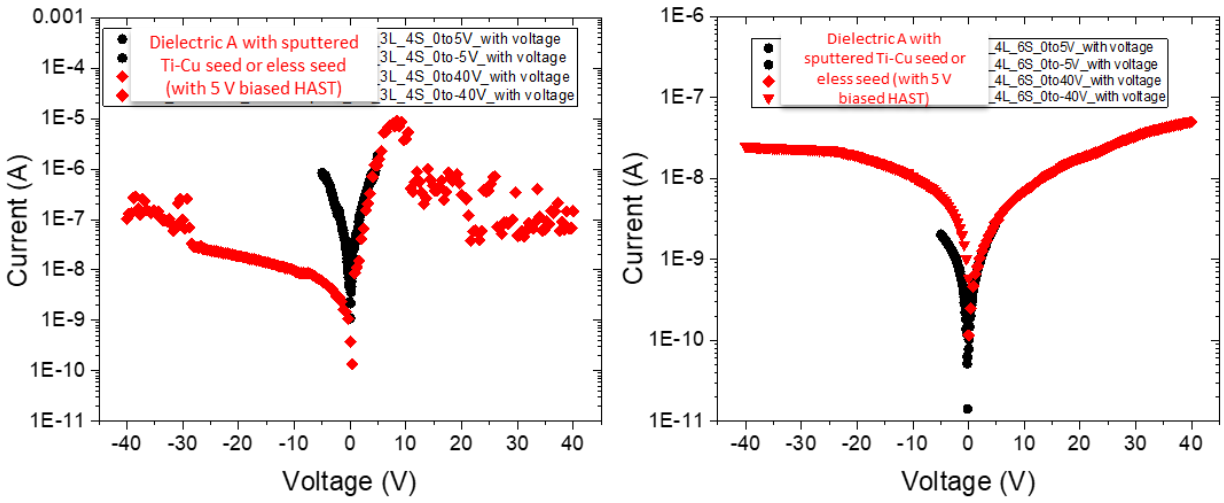


Figure 7-7: Leakage current behavior of dielectric A with electroless or sputtered seed layer after 100 hours of biased HAST at 5V. The rough interfaces seem to have sparked and smoothened out with application of voltage and there are no sparks seen any more for electroless copper seed layer samples.

To predict the maximum allowed moisture absorption of polymer dielectric required to pass < 2 µm space RDL electrochemical migration failures, there is a need to develop a model with the existing polymer dielectric of 0.6 wt. % moisture absorption which is advanced in terms of very low halogen content (< 10 ppm). The Peck, Eyring and Hornung models have been chosen as references to come up with a basic equation as shown below [[48], [49], [50], [51]].

$$t_f = \alpha * f(G) * V^{-m} * RH^{-n} * \exp(-\frac{\Delta H}{kT}) \qquad \textbf{Eq. (7-1)}$$

In this equation, t_f is the time to failure, α is a proportionality constant, f (G) is the function of spacing between electrodes, V is the applied voltage, RH is the relative humidity, ΔH is the activation energy, k is Boltzman's constant and T is the applied temperature. The constants n, m and ΔH need to be experimentally determined for the polymer dielectric. Samples with copper-polymer dielectric insulator-copper structure is fabricated with the thickness of dielectric in the

range of 7 µm. This is shown in Figure 7-8. The samples are exposed to varying levels of humidity (75 %, 85 %, 95 %) and voltage (5V, 10V and 20V) to predict some of the unknowns in the model.

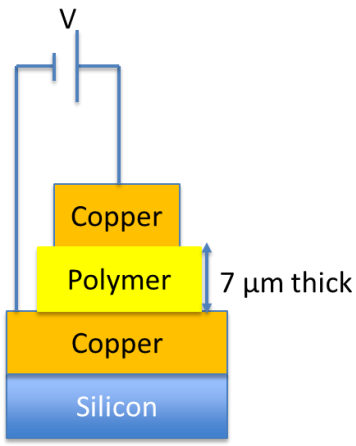


Figure 7-8: Copper-polymer-copper structure to study electrochemical migration failure through 7 µm thick polymer dielectric

Three different dielectrics X, Y and Z were evaluated for this study and all the three dielectrics were epoxy-based resins with different silica filler content. The moisture absorption of these dielectrics was measured by gravimetric analysis using a weighing scale with a minimum measurable weight of 0.0001 mg. The samples were soaked for 24 hours at 95 ^{0}C in water and the moisture absorption of the dielectrics are summarized in Table 7-1.

Table 7-1: Moisture absorption of different dielectrics (24 hours @ 95 ^{0}C in water)

Dielectric Type	Moisture absorption (wt.%)
X	1.1
Y	0.6
Z	0.25

The leakage current behavior of dielectric X and dielectric Z shown in Figure 7-9 indicates that for higher moisture absorption dielectric X, the leakage currents are higher after 150 hours of unbiased HAST.

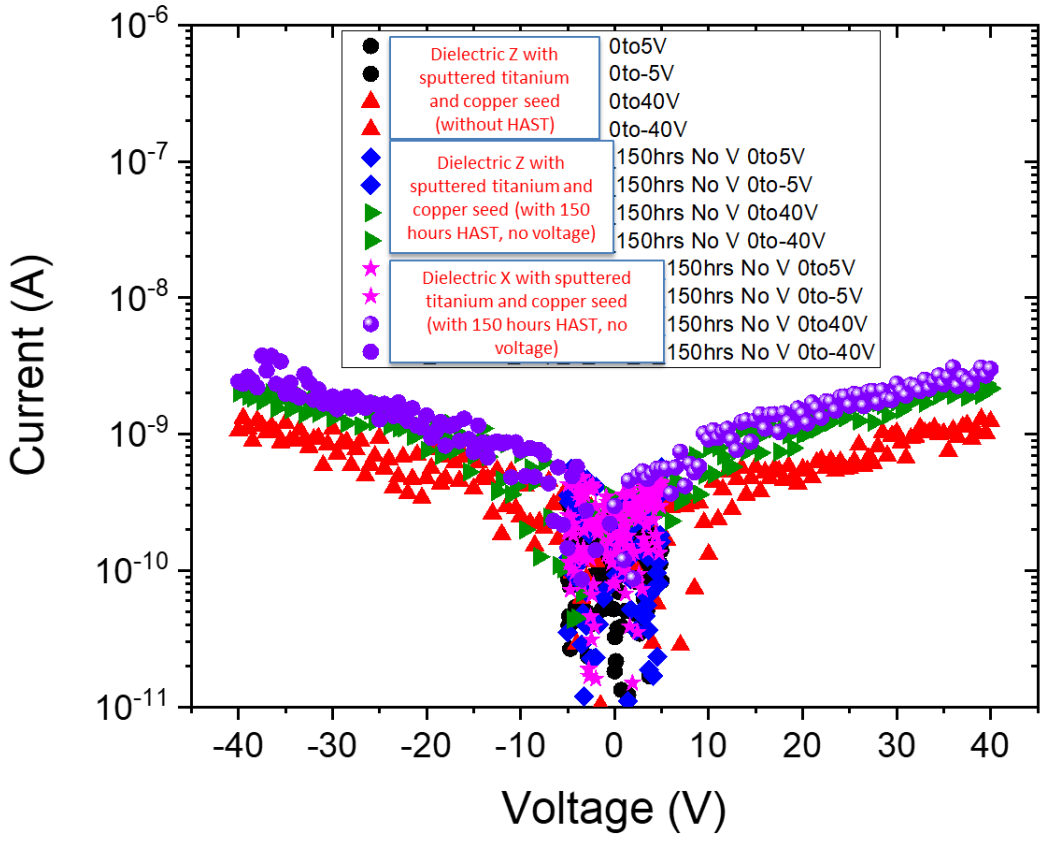


Figure 7-9: Leakage current behavior of dielectrics X and Z with 150 hours of HAST (No bias voltage was applied)

To study the dependence of time to failure on voltage, the samples of dielectric Y were exposed to 5V, 10 V and 20 V and the times to failure were recorded. In this case, failure was a complete electrical short (insulation resistance less than 1 kΩ). The times to failure are shown in Table 7-2 and the results show that the time to failure is proportional to the applied voltage with power of $V^{-1.5 \text{ to } -2}$.

Table 7-2: Time to failure for dielectric Y for varying voltage levels

Applied Voltage (in Volts)	Experimentally measured time to failure (in hours)
5	160
10	65
20	16

To study the dependence on relative humidity, the dielectric Y was exposed to 75%, 85 % and 95 % RH and the time to failure was found to be proportional to the relative humidity with power of RH^{-3}. The equation (7-1) becomes:

$$t_f = \alpha * f(G) * V^{-1.5\ to\ -2} * RH^{-3} * \exp(-\frac{\Delta H}{kT}) \qquad \textbf{Eq. (7-2)}$$

The function f(G) could not be calculated as these dielectrics were filled with silica fillers and the path of moisture to reach the dielectric is highly dependent on the distribution of silica fillers inside the dielectric. Three different dielectric thicknesses were studied, but there was no direct correlation of time to failure with thickness of the dielectric. This was also confirmed with a study to experimentally measure different line width (L) and space (S) structures using the same polymer dielectric with different seed layer treatments. There was no specific correlation for time to failure with varying space dimensions between copper RDL structures for 2 µm L/S, 3 µm L/S, 5 µm L/S and 7 µm L/S using the same polymer dielectric for all cases [61]. This is shown in Table 7-3.

Table 7-3: Time to failure (in hours) under biased HAST condition (1300C, 85% RH, 3.5V) for varying line width and space copper RDL structures with the same polymer dielectric for different seed layer treatments (marked as numbers 2-6) [61]

L/S [μm]	No.2	No.3	No.4	No.5	No.6
2/2	Pass	30 (7)	11 (5)	22 (1)	19 (20)
3/3	Pass	90 (4)	20 (2)	40 (3)	49 (11)
5/5	Pass	94 (2)	127 (17)	140 (13)	86 (1)
7/7	Pass	169 (2)	134 (18)	Pass	Pass

The dielectrics X and Z were tested at 20 V. A correlation of moisture absorption (in wt.%) for a dielectric to the atmospheric relative humidity (%) was established by Michael Pecht et. al. as shown in Figure 7-10 [62]. Based on this, an assumption was made to correlate the moisture absorption of dielectric Y (0.6 wt.%) would be equivalent to 80 % RH while dielectric Z with a moisture absorption of 0.25 wt.% would be equivalent to 50 % RH. Using the cubic factor of RH proportionality, the predicted time to failures were calculated keeping dielectric Y as a reference. This is shown in Table 7-4. Since all the three dielectrics were epoxy-based, the activation energies of these dielectrics (~ 1 eV) are around the same range. However, there were some deviations from the predicted model. This can be due to variations in the thicknesses of dielectrics or due to the pathway of copper oxide particles being different due to the silica filler distribution.

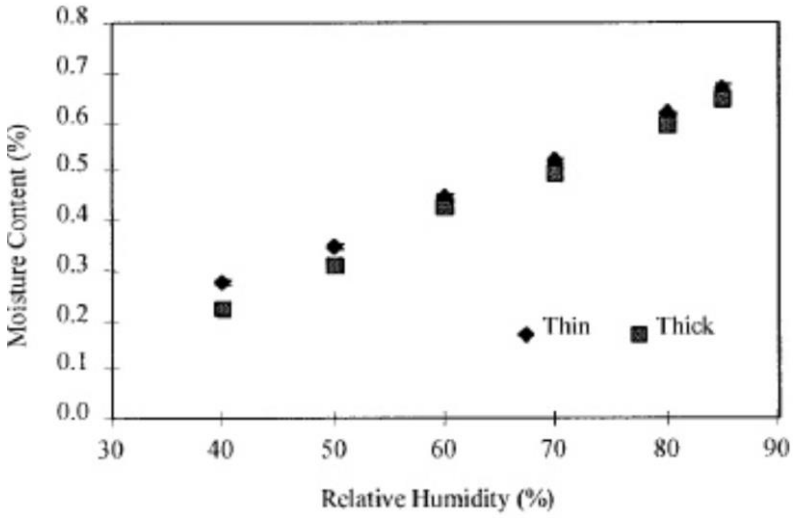


Figure 7-10: Correlation of moisture absorption of a dielectric to the relative humidity (%) in its atmosphere [62]

Table 7-4: Experimentally measured and predicted time to failures using moisture absorption- relative humidity correlation [62]

Dielectric	Moisture absorption (wt.%)	Equivalent Relative Humidity (%) [62]	Predicted time to failure (in hours) (from equation (7-2) assuming all other factors as equal)	Experimentally measured time to failure (in hours)
X	1.1	130 %	3.7	2
Y	0.6	80 %	16 (experimentally measured taken as a reference)	16
Z	0.25	45 %	89.9	60

Thus, a dielectric with moisture absorption of 0.25 wt.% can introduce a 3-4X increment in time to failure for electrochemical migration of copper compared to a dielectric with moisture absorption of 0.6 wt.%. Based on the results shown in Figure 7-6, a dielectric with moisture absorption of 0.25 wt.% will result in the required > 200 hours of biased HAST life for polymer RDL with 1.5 µm space structures. With parylene-F as a passivation layer as described in Figure 6-12 and the moisture absorption of parylene-F being < 0.1 wt.%, the time to failure can be

extended to more than 1000 hours. The function f(G), being unknown, the ideal thickness of parylene-F required as a passivation barrier cannot be predicted. In the future studies for sub1-micron RDL, this part needs to be empirically studied with a large number of sample sets.

7.2 Thermal cycling reliability of 2-3 µm diameter microvias with polymer RDL

The thermal cycling reliability of microvias in polymer dielectrics is studied using building daisy chain test structures of about 400 microvias. The samples are exposed to pre-conditioning followed by air-to-air thermal cycling as per JEDEC JESD22- A104D (Hold time of 15 mins at each temperature -55 ^{0}C and 125 ^{0}C with transition time from -55 ^{0}C to 125 ^{0}C being 15 mins). The electrical resistances of the daisy chain structures are measured using a four-probe test and any change in electrical resistance > 10% is considered to be failed. Figure 7-11 shows the cross-Kelvin bridge structure to measure contact resistance of a single microvia on the left and a cross section of the daisy chain of microvias with each microvia geometry being 4 µm (top diameter) and 2 µm (bottom diameter) microvia at a via depth of 2 µm [Aspect ratio is 0.5 and taper angle is 64^0]. The polymer dielectric is the novel nano-silica filled photosensitive epoxy dielectric discussed in section 5.2.1 with low CTE (35 ppm/K) and moderately good tensile strength (95 MPa) and % elongation to break (6 %) measured at room temperature. The structure is expected to pass ~1900 thermal cycles of reliability with 64^0 taper angle microvia structure. The results in Figure 7-12 confirm the modeling results. The test was run with a high CTE (45 ppm/K) dielectric with lower tensile strength of 85 MPa measured at room temperature. The results in Figure 7-13 confirm the modeling results showing polymer cracks after 100 thermal cycles.

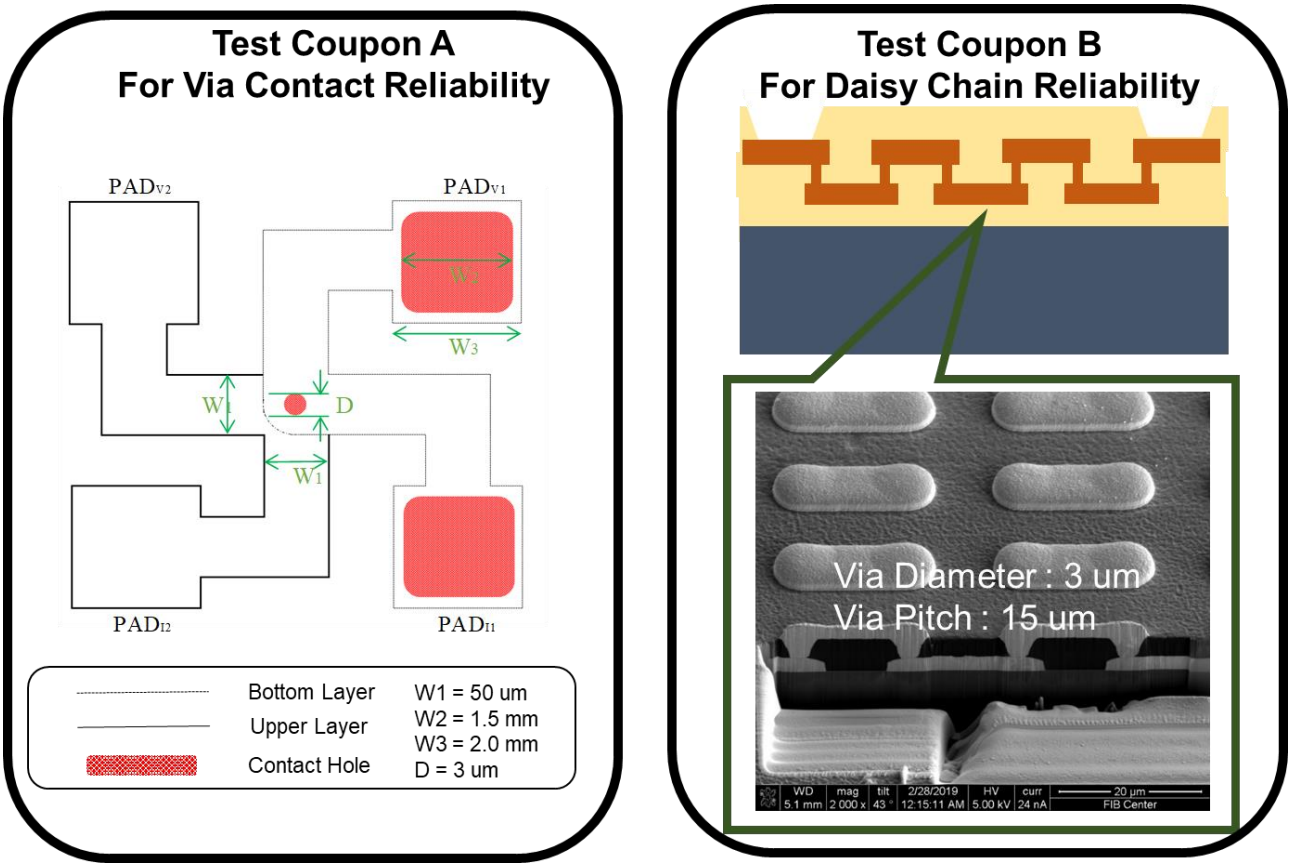


Figure 7-11: Kelvin structure (Left) to test contact resistance of single microvia and daisy chain structure (Right) of 400 microvias to test microvia reliability

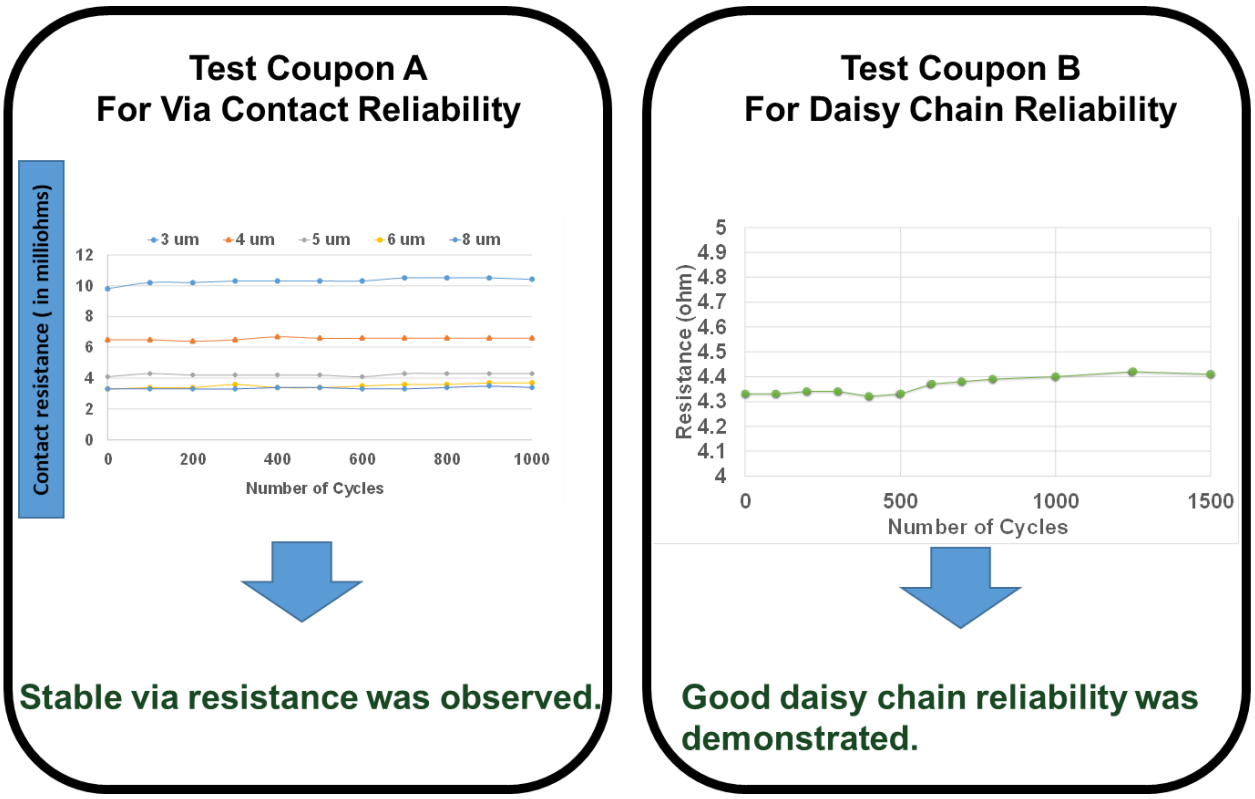


Figure 7-12: Results of contact resistance and thermal cycling reliability of microvia daisy chain. The dielectric is able to survive > 1500 cycles as predicted by model [Section 5.2.1 and Table 5-7]

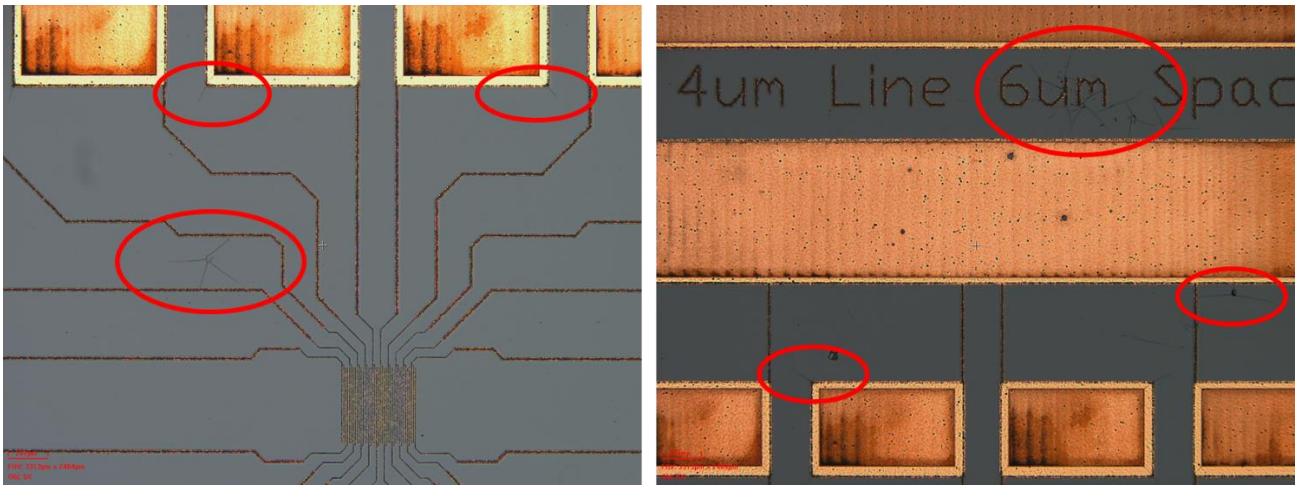


Figure 7-13: Post-thermal cycling (after 100 cycles) crack in high CTE (45 ppm/K at room temperature) polymer dielectric with low tensile strength (85 MPa at room temperature)

7.3 Chapter 7 Summary

This chapter demonstrates two aspects of reliability: (A) Electrochemical migration reliability of 1.5 µm to 3 µm space copper RDL comb structures with polymer dielectrics under biased HAST and, (B) Thermal cycling reliability of 2 µm bottom diameter photovias. In part (A), the study identifies the need for lower moisture absorption polymer dielectrics and using a moisture absorption-relative humidity correlation model, the study predicts and validates 3-4X increment in time to failure using a 0.25 wt.% moisture absorption dielectric compared to 0.6 wt.% moisture absorption polymer dielectric. With a 0.6 wt.% moisture absorption polymer dielectric, the time to failure for 1.5 µm space copper RDL structure was ~ 80 hours. Thus, a 0.25 wt. % moisture absorption polymer dielectric can reliably pass > 200 hours of biased HAST at 1.5 µm space copper RDL structures. For part (B), the thermal cycling reliability of 2 µm bottom diameter photovias is demonstrated using the ideal low CTE polymer dielectric developed in section 5.2.1.

CHAPTER 8. SUMMARY AND FUTURE WORK

This dissertation presented the first comprehensive research on 2 µm multi-layer polymer RDL in five different aspects for 2.5D glass substrates for high performance computing applications:

(A) Modeling for layer-to-layer registration to predict the fundamental capture pad required for laminate versus glass core material

(B) Design for high bandwidth, low delay polymer RDL compared to silicon BEOL RDL

(C) Advanced materials for 2 µm multi-layer polymer RDL

(D) Advanced processes for 2 µm multi-layer polymer RDL

(E) Reliability of 2 µm multi-layer polymer RDL

Silicon interposers with 1-2 µm RDL are currently being used for high performance computing applications. These are limited by high resistance and high capacitance due to SiO_2 BEOL RDL, limiting the bandwidth scaling beyond 2 Gbps per signal channel. The challenges with laminate core materials in terms of dimensional stability requiring larger capture pads and materials and process issues to fabricate < 5 µm RDL with reliability prevent the adoption of low cost, panel scale substrates with polymer RDL. This research addresses these challenges to scale polymer RDL to be used with advanced laminate or glass substrates with novel design, materials, processes and reliability studies.

8.1 Research Summary

Task 1: Modeling for layer-to-layer registration for laminate versus glass core materials

A deep understanding of the parameters affecting the dimensional change in core materials have been established. The minimum capture pad required for laminate and glass core materials was established in this study. Finite element modeling was used to predict the dimensional changes

in laminate core materials with varying CTE and elastic modulus and low CTE and high CTE glass core materials for varying copper area density patterns. Experimental characterization was performed to predict the shrinkage due to post-curing process laminate core materials.

Task 2: Design for high bandwidth, low delay 2 µm multi-layer polymer RDL

The design for 2 µm multi-layer RDL was compared with a bump and signal channel geometric structure for polymer versus SiO_2 RDL. Both stripline and embedded microstrip transmission line structures at 6 mm line lengths were used for the simulations. The design simulations concluded that glass-based polymer RDL can handle higher data rate per signal channel due to the low capacitance of polymer dielectric. An aspect ratio of 0.5 for fixed 2 µm line width and 2 µm space structure was found to be optimum for the highest bandwidth performance for both stripline and embedded microstrip line configurations. For stripline configuration, the best eye performance was for aspect ratio of 4.2 with a line width of 0.5 µm and space of 5 µm for a dielectric thickness of 3 µm while for embedded microstrip line, aspect ratio of 0.5 with a line width of 0.7 µm and space of 4.6 µm for top dielectric thickness of 1.7 µm and bottom dielectric thickness of 1 µm showed the best eye performance. Thus, there was a need to develop materials and processes for aspect ratios of upto 4 for future high bandwidth RDL. With this optimized design RDL, the glass polymer RDL can deliver 5X higher bandwidth at 3X lower latency for signal channels.

Task 3: Materials for 2 µm multi-layer polymer RDL

This study focused on using novel chemically amplified, positive tone dry film photoresists to pattern up to 1 µm RDL with aspect ratios of up to 5. The second part focused on designing polymer dielectrics for thermal (CTE), mechanical (% elongation to break, tensile strength and

elastic modulus) for fabrication of reliable 2 µm diameter microvias. As polymer dielectrics are scaled to smaller microvia diameters, the taper angles of the microvias become in the range of 55^0-75^0. This presents significant challenges in the cracking of copper as well as polymer dielectrics at negative temperatures of cycling. This led to evaluation of five major classes of polymer dielectrics being used today for three-layer stacked microvia reliability and identify the ideal properties of polymer dielectrics for fabrication of reliable microvias. A novel low CTE polymer dielectric with nano-silica filler having moderately good tensile strength and % elongation to break properties was identified and capable of resolving < 5 µm diameter microvias. The last part of this study focused on designing polymer dielectric for superior interfacial adhesion of sputtered titanium seed to polymer dielectric. The presence of phenoxy group in polymer dielectric was identified to result in excellent peel strength of sputtered Ti-Cu seed to polymer dielectric. The required peel strength for 2 µm RDL was also identified with finite element modeling for varying aspect ratio of copper lines using low CTE and high CTE polymer dielectrics.

Task 4: Processes for 2 µm multi-layer polymer RDL

This study discussed about semi-additive process and its challenges in seed layer etch process to scale to 2 µm RDL. Embedded trench RDL using photosensitive dielectric and excimer laser based embedded trench RDL using non-photosensitive dielectric was evaluated. The challenges in planarization for embedded trench RDL were identified and the need for a novel zero-side etch process to scale SAP RDL was identified. A novel process using a parylene barrier was demonstrated with zero side-etch to scale SAP RDL even to sub 1-micron RDL. Microvia processes to scale diameters below 5 µm with vertical taper angles (close to 90^0) were found to have a very tight process window. Also, the limitation of a minimum 2 µm bottom diameter of microvia was observed for both photosensitive dielectrics and excimer laser drilled non-

photosensitive dielectrics. Thus, a novel process flow was demonstrated to scale microvia diameters to even sub 1-micron dimensions using photoresist patterning instead of dielectric patterning.

Task 5: Reliability of 2 µm multi-layer polymer RDL

This study discussed two aspects of reliability: (A) Electrochemical migration reliability of 1.5 µm and 3 µm space copper RDL structures using polymer dielectrics with varying wt.% moisture absorption and, (B) Thermal cycling reliability of 2-3 µm diameter photovias. The study identified the need for a lower moisture absorption polymer dielectric to pass biased HAST for 1.5 µm space copper structures. The sample with 0.6 wt.% moisture absorption failed biased HAST within ~ 80 hours for 1.5 µm space copper RDL structures. Time to failure was found to be proportional to the cubic power of relative humidity for electrochemical migration. Using a moisture absorption-relative humidity correlation model, the time to failure for a 0.25 wt.% moisture absorption polymer dielectric was found to increase by a factor of 3-4X compared to a 0.6 wt.% moisture absorption polymer dielectric. For part (B), the thermal cycling reliability of 2 µm bottom diameter photovias is demonstrated using the ideal low CTE polymer dielectric developed in section 5.2.1.

8.2 Scientific and Technological Contributions

The following is a list of contributions of this dissertation.

- Modeled layer-to-layer registration to predict the minimum capture pad diameter for landing a microvia comparing different CTE and modulus laminate core and glass core materials.

- Designed 2 µm multi-layer polymer RDL and proposed a stack-up for higher signal data rates (upto 5X) and lower latency (3X) compared to silicon BEOL RDL using stripline and embedded microstrip transmission line models.

- Material design for thermal and mechanical properties of polymer dielectrics for fabrication of reliable 2 µm microvia structures.

- Analyzed bonding mechanism of titanium sputtered seed to smooth polymer dielectrics. The need for a higher peel strength was identified with high aspect ratio RDL and phenoxy functional group in polymer dielectric was confirmed to have superior peel strength with sputtered titanium seed.

- Demonstrated a novel process for zero side-etch during seed layer removal step and for scaling polymer RDL to sub 1- micron microvia diameters using photoresist materials to scale semi-additive processes (SAP) for future polymer RDL

- Analyzed electrochemical migration failures in fine space copper RDL structures with varying moisture absorption polymer dielectrics. The need for a lower moisture absorption (0.25 wt.%) polymer dielectric was identified for 1.5 µm space copper RDL structures. Demonstrated thermal cycling reliability of 2 µm bottom via diameter photovias.

8.3 Future Work

This dissertation has raised many new challenges for further research to scale polymer RDL to sub 1-micron dimensions. The first topic is the photolithography process and tools required to scale multi-layer RDL to sub 1-micron features at panel scales with large field exposures and high depth of focus (DoF). The dissertation has identified the optimum design of 0.5 µm line width with an aspect ratio of 4.2 using a dielectric with D_k = 2.4 to achieve > 5X bandwidth for glass-based polymer RDL compared to silicon RDL with 3X lower latency. The second topic is to demonstrate

stacked 1-micron diameter microvia reliability using the novel process flow developed in this thesis. The polymer dielectric with the right set of properties have been identified in this dissertation for fabrication of reliable microvias. The last topic is to evaluate the leakage behavior of a low moisture polymer dielectric system with parylene-F as a passivation barrier at < 1 μm copper RDL structures to prevent electrochemical migration failures during biased HAST.

REFERENCES

[1]. Gordon Moore; International Electron Devices Meeting, Technical Digest, IEEE (1975)

[2]. Tummala, Rao R., and Eugene J. Rymaszewski, eds., *Microelectronics packaging handbook*. Vol. 16. New York: Van Nostrand Reinhold, 1989.

[3]. Mark Lapedus, "Transistor options beyond 3 nm," https://semiengineering.com/transistor-options-beyond-3nm/, February 15, 2018

[4]. M. Ishida, "APX (Advanced Package X) - Advanced Organic Technology for 2.5D Interposer," in *2014 CPMT Seminar, Latest Advances in Organic Interposers*, Lake Buena, Vista, Florida, USA, May 27-30, 2014.

[5]. Rao, Vempati Srinivasa, Chai Tai Chong, David Ho, Ding Mian Zhi, Chong Ser Choong, Sharon Lim PS, Daniel Ismael, and Ye Yong Liang. "Development of high density fan out wafer level package (HD FOWLP) with multi-layer fine pitch RDL for mobile applications," In *2016 IEEE 66th Electronic Components and Technology Conference (ECTC)*, pp. 1522-1529. IEEE, 2016.

[6]. K. Oi, S. Otake, N. Shimizu, S. Watanabe, Y. Kunimoto, T. Kurihara, T. Koyama, M. Tanaka, L. Aryasomayajula and Z. Kutlu, "Development of New 2.5D Package with Novel Integrated Organic Interposer Substrate with Ultra-fine Wiring and High-Density Bumps," *2014 IEEE 64th Electronic Components and Technology Conference*, Lake Buena, Vista, FL, USA, pp. 348-353, May 27–30, 2014.

[7]. Young Do Kweon, "Low Cost Solutions for 2.5D Packaging", Samsung Electro-Mechanics, MEPTEC, Nov 2012, http://meptec.org/Resources/10%20-%20Samsung.pdf

[8]. Kudo, Hiroshi, Ryohei Kasai, Jyunichi Suyama, Mitsuhiro Takeda, Yumi Okazaki, Haruo Iida, Daisuke Kitayama et al. "Demonstration of High Electrical Reliability of Sub-2 Micron Cu Traces Covered with Inorganic Dielectrics for Advanced Packaging Technologies." In *2017 IEEE 67th Electronic Components and Technology Conference (ECTC)*, pp. 1849-1854. IEEE, 2017.

[9]. Islam Salama, "Continuum Computing Enabling IC Scaling, Miniaturization and System Integration through Advanced Packaging," The ConFab 2016, http://theconfab.com/wp-content/uploads/PRES_IslamSalama.pdf

[10]. R. Mahajan, R. Sankman, N. Patel, D-W Kim, K. Aygun, Z. Qian, Y. Mekonnen, I. Salama, S. Sharan, D. Iyengar, and D. Mallik, "Embedded Multi-Die Interconnect Bridge (EMIB) – A High Density, High Bandwidth Packaging Interconnect," *2016 IEEE 66th Electronic Components and Technology Conference*, Las Vegas, Nevada, USA, pp.557-565, May 31-June 3, 2016.

[11]. Andy Heinig, "Technology Options and Their Influence on Routing for Interposer-based Memory Processor Integration," January 28, 2015, https://www.3dincites.com/2015/01/technology-options-influence-routing-interposer-based-memory-processor-integration/

[12]. Performance Characteristics of IC Packages, 2000 Packaging Databook, Intel

[13]. Yole Développement, "Polymer Dielectrics for Advanced Packaging at the Wafer-Level," Slide 23, 2018.

[14]. Yuya Suzuki, "Ultra-thin polymer dielectric materials and ultra-small via and trench processes for 20-micron bump pitch re-distribution layer (RDL) structures for high density packages," Ph.D Dissertation, Georgia Institute of Technology, December 2017

[15]. Attila Geczy, Márta Fejos, László Tersztyánszky, "Investigating and compensating printed circuit board shrinkage induced failures during reflow soldering," Journal of Soldering & Surface Mount Technology, Volume 2, Issue 2, pp. 61-68, 2015

[16]. Rudajevova A., Dusek K., "Influence of Manufacturing Mechanical and Thermal Histories on Dimensional Stabilities of FR4 Laminate and FR4/Cu-Plated Holes," Journal of Materials, Volume 11, Issue 11, 2018.

[17]. Wickham M, Zou L, Hunt C, "An assessment of the suitability of current PCB laminates to withstand lead-free reflow profiles," NPL Report MATC(A)91, April 2002

[18]. Ushio Inc., "UX-series Ushio photolithography tools," https://www.ushio.co.jp/documents/products/lithography/UX_E_130524.pdf, https://www.ushio.com/product/large-field-stepper-ux5-ux7/

[19]. Suresh Ramalingam, "HBM Package Integration: Technology Trends, Challenges and Applications," Hot Chips, August 21, 2016, https://www.hotchips.org/wp-content/uploads/hc_archives/hc28/HC28.21-Tutorial-Epub/HC28.21.1-Next-Gen-Memory-Epub/HC28.21.141-HBM-package-Suresh_Ramalingam-Xilinx-v5.pdf

[20]. Cho, Kyungjun, Youngwoo Kim, Hyunsuk Lee, Jinwook Song, Junyong Park, Seongsoo Lee, Subin Kim, Gapyeol Park, Kyungjune Son, and Joungho Kim. "Signal integrity design and analysis of differential high-speed serial links in silicon interposer with through-silicon via," *IEEE Transactions on Components, Packaging and Manufacturing Technology* 99 (2018): 1-15.

[21]. Martwick, Andrew, and John Drew. "Silicon interposer and TSV signaling," In *2015 IEEE 65th Electronic Components and Technology Conference (ECTC)*, pp. 266-275. IEEE, 2015.

[22]. Lu, Hao, Yutaka Takagi, Yuya Suzuki, Brett Sawyer, Robin Taylor, Venky Sundaram, and Rao Tummala. "Demonstration of 3–5 μm RDL line lithography on panel-based glass interposers," In *2014 IEEE 64th Electronic Components and Technology Conference (ECTC)*, pp. 1416-1420. IEEE, 2014.

[23]. Hirohisa Narahashi, "Low D_f Build-up Material for High Frequency Signal Transmission of Substrates," The 63rd Electronic Components and Technology Conference (ECTC), The Cosmopolitan of Las Vegas, Nevada, USA, May 28 - 31, 2013

[24]. Jeffrey Gottro, "Polymers in Electronics Part Seven: Redistribution Layers for Fan-Out Wafer Level Packaging," May 8, 2017, https://polymerinnovationblog.com/polymers-electronics-part-seven-redistribution-layers-fan-wafer-level-packaging/

[25]. Processing procedures for CYCLOTENE 4000 Series Photo BCB Resins, February 2005, http://msdssearch.dow.com/PublishedLiteratureDOWCOM/dh_096d/0901b8038096dae3.pdf

[26]. Processing guidelines for ALX dielectric polymer, Dec 2010, http://fast.auburn.edu/wiki/images/e/ee/ALX_Data_Sheet.pdf

[27]. Takahiro Sasaki," Low temperature curable polyimide for advanced package," SEMICON Taiwan, September 2-4, 2015, http://www.semicontaiwan.org/zh/sites/semicontaiwan.org/files/data15/docs/6_5._20150902e5ss_semicontaiwan.pdf

[28]. Yamanaka Kimihiro, Teruya Fujisaki, Manabu Ichinose, and Takafumi Ooyoshi, "Effect of geometry and dielectric material on thermo-mechanical strain on micro-vias in build-up substrates," *Journal of Materials Science: Materials in Electronics* 21, no. 9 (2010): 943-949.

[29]. Lesniewski Thomas, "Effects of dielectric material, aspect ratio and copper plating on microvia reliability," In *Proc. IPC APEX Technical Conference*, pp. 25-27. 2014.

[30]. Mahalingam, Saketh, Shashikant Hegde, Gnyaneshwar Ramakrishna, Raghuram V. Pucha, and Suresh K. Sitaraman. "Material interaction effects in the reliability of high density interconnect (HDI) boards," In *ASME 2003 International Mechanical Engineering Congress and Exposition*, pp. 165-170. American Society of Mechanical Engineers, 2003.

[31]. G. Ramakrishna, L. Fuhan, and S. K. Sitaraman, "Role of dielectric material and geometry on the thermo-mechanical reliability of microvias," in Electronic Components and Technology Conference, 2002. Proceedings. 52nd, 2002, pp. 439-445.

[32]. Suzuki, Yuya, Ryuta Furuya, Venky Sundaram, and Rao R. Tummala. "Demonstration of 10-micron Microvias in Thin Dry-Film Polymer Dielectrics for High-Density Interposers," *IEEE Transactions on Components, Packaging and manufacturing technology* 5, no. 2 (2015): 194-200.

[33]. Ho, S. W., L. Ding, Song How Lim, Soon Ann Sek, Mingbin Yu, and G. Q. Lo. "Polymer-based fine pitch Cu RDL to enable cost-effective re-routing for 2.5 D interposer and 3D-IC," In *2013 IEEE 15th Electronics Packaging Technology Conference (EPTC 2013)*, pp. 435-439. IEEE, 2013.

[34]. Bernhard, Tobias, Simon Bamberg, Frank Brüning, Ralf Brüning, Laurence J. Gregoriades, Tanu Sharma, Delilah Brown, M. Klaus, and Ch Genzel, "Analysis of stress/strain in Electroless Copper Films," In *International Symposium on Microelectronics*, vol. 2013, no. 1, pp. 000026-000030. International Microelectronics Assembly and Packaging Society, 2013.

[35]. Jonas Barth, "Intrinsic stress in thin metallic multilayers," Master of Science Thesis, Tampere University of Technology, February 2018

[36]. John Hunt, "FanOut- Simple to Complex," SEMICON Taiwan, http://semicontaiwan.org/zh/sites/semicontaiwan.org/files/data16/docs/6.%20ASE_John%20Hunt.pdf

[37]. Kim Jinyoung, Ikjun Choi, JunHyeong Park, Jae-Ean Lee, TaeSung Jeong, Jungsoo Byun Young, Gwan Ko, Kangheon Hur, Dae-Woo Kim, and Kyung Suk Oh, "Fan-out Panel Level Package with Fine Pitch Pattern," In *2018 IEEE 68th Electronic Components and Technology Conference (ECTC)*, pp. 52-57. IEEE, 2018.

[38]. Thomas, Thomas. "Development of a New Adhesion Promoter for Metal Adhesion on Polymer Substrates for Printed Circuit Board Production Using Functionalized Silica Nanoparticles." PhD diss., 2016.

[39]. Bernt, Marvin, Paul Van Valkenburg, David Surdock, and Prayudi Lianto. "Enabling a Robust Copper Seed Etch Process for Fine Line RDL by Electroplating on a Thin PVD Seed Layer." In *International Symposium on Microelectronics*, vol. 2018, no. 1, pp. 000207-000211. International Microelectronics Assembly and Packaging Society, 2018.

[40]. Michalik F., N. Luetzow, G. Schmidt, T. Huelsmann, M. Kloppisch, R. Haidar, and P. Brooks. "EcoFlash™: Next level of enhanced isotropic etchants." In *2015 10th International Microsystems, Packaging, Assembly and Circuits Technology Conference (IMPACT)*, pp. 83-87. IEEE, 2015.

[41]. Suzuki Yuya, Venky Sundaram, Rao Tummala, Habib Hichri, Lee Seongkuk, Markus Arendt, Ye Chen et al. "Embedded Trench Redistribution Layers (RDL) by Excimer Laser Ablation and Surface Planer Processes." In *2017 IEEE 67th Electronic Components and Technology Conference (ECTC)*, pp. 884-889. IEEE, 2017

[42]. Shi, Tailong, Chintan Buch, Vanessa Smet, Yoichiro Sato, Lutz Parthier, Frank Wei, Cody Lee, Venky Sundaram, and Rao Tummala. "First demonstration of panel glass fan-out (GFO) packages for high I/O density and high frequency multi-chip integration." In *2017 IEEE 67th Electronic Components and Technology Conference (ECTC)*, pp. 41-46. IEEE, 2017.

[43]. Wei, Frank, Vanessa Smet, Ninad Shahane, Hao Lu, Venky Sundaram, and Rao Tummala. "Ultra-Precise Low-Cost Surface Planarization Process for Advanced Packaging Fabrications and Die Assembly: A Survey of Recent Investigations on Unit Process Applications and Integrations." In *2016 IEEE 66th Electronic Components and Technology Conference (ECTC)*, pp. 1740-1745. IEEE, 2016.

[44]. Okamoto, Daichi, Yoko Shibasaki, Daisuke Shibata, Tadahiko Hanada, Fuhan Liu, Venky Sundaram, and Rao R. Tummala. "An Advanced Photosensitive Dielectric Material for High-Density RDL with Ultra-Small Photo-Vias and Ultra-Fine Line/Space in 2.5 D Interposers and Fan-Out Packages." In *2018 IEEE 68th Electronic Components and Technology Conference (ECTC)*, pp. 1543-1548. IEEE, 2018.

[45].Cho Taiheui, and Paul Ho, "Thermal and bias-temperature stress induced leakage current failure of Cu/BCB single Damascene integration." In *Extended abstracts of the... Conference on Solid State Devices and Materials*, vol. 1998, pp. 268-269. 1998.

[46]. Kanki, Tsuyoshi, Junya Ikeda, Yasushi Kobayashi, Shoichi Suda, Yoshihiro Nakata, and Tomoji Nakamura. "Highly Reliable Chip to Chip wiring technology by using barrier material with high anti-corrosion property for 3D/2.5D- IC," Vol. J96-C, No. 11, pp. 379-386.

[47]. Tsuyoshi Kanki, Junya Ikeda, Yoshihiro Nakata, Motoaki Tani, And Tomoji Nakamura, "Development of highly reliable fine wiring technology applying semiconductor process," *Journal of Japan Institute of Electronics Packaging*, no. 6 (2015): 435-442.

[48]. Elissa Bumiller and Dr. Craig Hillman, "A Review of Models for Time-to-Failure Due to Metallic Migration Mechanisms," White Paper, https://www.dfrsolutions.com/hubfs/DfR_Solutions_Website/Resources-Archived/White-Papers/Reliability/Review-of-Models-for-Time-to-Failure-Due-to-Metallic-Migration-Mechanisms.pdf

[49]. A. Hornung, "Diffusion of silver in borosilicate glass," Proceedings of the 1968 Electronic Components Conference. New York, NY, USA: IEEE, 1968. pp. 250-5

[50]. D.S. Peck, "Comprehensive Model for Humidity Testing Correlation," IEEE IRPS Proceedings, 1986. pp. 44 – 50.

[51]. D.S. Peck and O. Hallberg, "Recent, humidity accelerations, a base for testing standards," Quality and Reliability Engineering International, vol.7, no.3, May-June 1991. pp. 169-180

[52]. Dynamic Mechanical Analysis, A Beginner's Guide, https://www.perkinelmer.com/CMSResources/Images/4474546GDE_IntroductionToDMA.pdf

[53]. Liu Fuhan, Chandrasekharan Nair, Hirokazu Ito, Bartlet H. DeProspo, Siddharth Ravichandran, Hisanori Akimaru, Koichi Hasegawa, and Rao R. Tummala. "Low Cost One Micron Photolithography Technologies for Large Body Size, Low Resistance Panel-Based RDL." *IEEE Transactions on Components, Packaging and Manufacturing Technology* (2019).

[54]. Goto, Yoshio, Kosuke Urushihara, Bunsuke Takeshita, and Ken-Ichiro Mori, "A study of Sub-micron Fan-out Wafer Level Packaging solutions: Canon," In *International Symposium on Microelectronics*, vol. 2018, no. 1, pp. 000488-000493. International Microelectronics Assembly and Packaging Society, 2018.

[55]. Lau, John H. "The future of interposer for semiconductor IC packaging." *Chip Scale Rev* 18, no. 1 (2014): 32-36.

[56]. Shimizu, Noriyoshi, Wataru Kaneda, Hiromu Arisaka, Naoyuki Koizumi, Satoshi Sunohara, Akio Rokugawa, and Toshinori Koyama. "Development of organic multi chip package for high performance application." In *International Symposium on Microelectronics*, vol. 2013,

no. 1, pp. 000414-000414. International Microelectronics Assembly and Packaging Society, 2013.

[57]. Nakamura, Shigeo, “PCB-OS Symposium Faster, reliable and lower cost electronics through innovative technology integration,” IBM Building 400 Research Triangle Park, NC, 2007.

[58]. Chang, Yu-Chen, Tz-Cheng Chiu, Yu-Ting Yang, Yi-Hsiu Tseng, Xi-Hong Chen, and Pu-Shan Huang. "Fatigue response of polyimide thin film under cyclic loading," In *2015 10th International Microsystems, Packaging, Assembly and Circuits Technology Conference (IMPACT)*, pp. 233-236. IEEE, 2015.

[59]. Arthur Keigler, Stephen Golovato, Kathy O’Donnell, Johannes Chiu, Richard Hollman, “PVD Processing for Flip-Chip: Considering Adhesion Layer Properties,” https://electroiq.com/2007/09/pvd-processing-for-flip-chip/

[60]. Liu Fuhan, Chandrasekharan Nair, Atsushi Kubo, Tomoyuki Ando, Frank Wei, Venky Sundaram, and Rao R. Tummala. "Organic Damascene Process for 1.5-Micron Panel-Scale Redistribution Layer Technology Using 5-Micron Thick Dry Film Photosensitive Dielectrics." *IEEE Transactions on Components, Packaging and Manufacturing Technology* 8, no. 5 (2018): 792-801.

[61]. Haruki Sueyoshi, Keita Furuhashi, Shigehiro Hayashi, Kanta Nogita, Younggun Han, Osamu Horiuchi, and Hajime Tomokage, “Reliability Evaluation of Ultra-Fine Copper Pattern by ElectroPlating,” IEICE Journal C, Vol. J99-C, Number 11 (2016), pp. 524-526.

[62]. Pecht, Michael G., Haleh Ardebili, Anand A. Shukla, John K. Hagge, and David Jennings. "Moisture ingress into organic laminates," *IEEE Transactions on Components and Packaging Technologies* 22, no. 1 (1999): 104-110.